

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) Publication number:

0 595 792 A2

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 94200046.4

(51) Int. Cl.⁵: G09G 3/30, G09G 3/36,
H04N 3/12

(22) Date of filing: 09.12.88

This application was filed on 11 - 01 - 1994 as a
divisional application to the application
mentioned under INID code 60.

(30) Priority: 07.06.88 JP 139638/88
02.07.88 JP 165561/88
18.07.88 JP 179997/88
18.07.88 JP 179998/88

(43) Date of publication of application:
04.05.94 Bulletin 94/18

(60) Publication number of the earlier application in
accordance with Art.76 EPC: 0 345 399

(84) Designated Contracting States:
DE GB

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(54) Method and apparatus for driving capacitive display device.

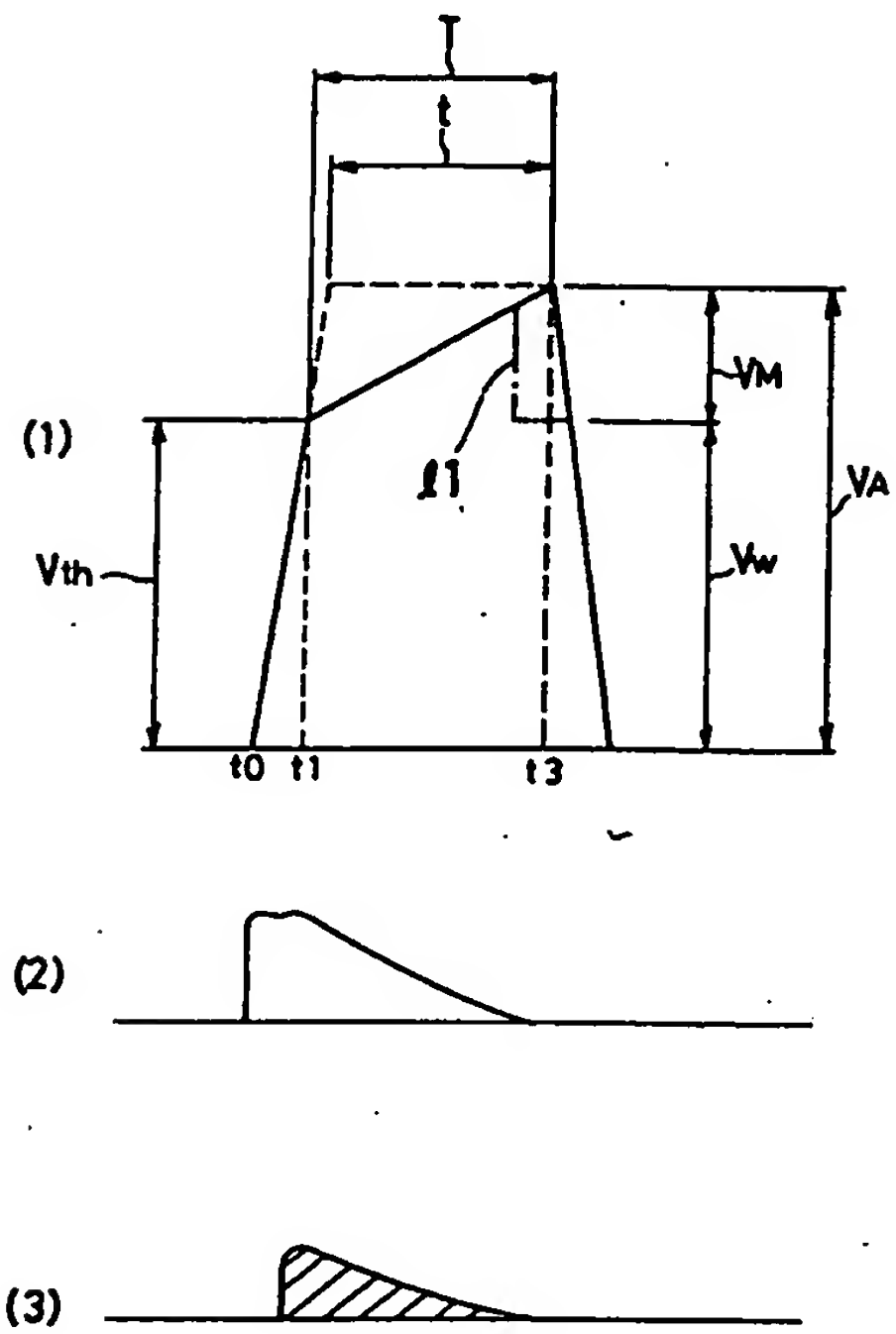
(57) This invention relates to gradation display by pulse width control method (PWM method) in each pixel in a capacitive display apparatus such as electroluminescent liquid crystal display apparatus. The driving voltage applied to the data electrodes is caused to vary in a ramp waveform, and the number of gradations of gradation display by the PWM method is increased. Since the capacitive display apparatus is used, the driving pulse is increasingly influenced by capacity as the location of the pixel to be controlled is further away from the drive circuit of the data electrode and in particular its duration becomes extended. As a result, even for identical gra-

dation data, uneven illumination may occur. In this invention, the pulse width applied to the data electrodes is gradually decreased as scanning of the electrodes progresses. Therefore, the brightness of the capacitive display apparatus may be made uniform over the entire screen surface.

Also, in the invention an impedance converting means connected in series between a DC power supply and the data electrodes is controlled by a control signal, with a switching means being controlled to effect application of a current to the data electrode for a period according to gradation display data.

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Fig.15



This invention relates to methods and apparatus for driving a capacitive display device such as an electroluminescent (EL) display device. In particular, the invention relates to driving for gradation display of individual pixels.

Capacitive displays are well known and can be fabricated in a number of ways. For instance, a double insulation type (or triple insulation structure) thin film EL element is composed as follows.

As shown in FIG. 1, parallel strips of transparent electrodes 2 made of In_2O_3 are disposed on a glass substrate 1. A layer 3a of an inductive substance such as Y_2O_3 , Si_3N_4 , Al_2O_3 or the like, an EL layer 4 made of ZnS doped with an activator such as Mn, and another layer 3b of a similar inductive substance of such as Y_2O_3 , Si_3N_4 , TiO_2 , Al_2O_3 or the like are sequentially laminated on the glass substrate 1. The film thickness is from 500 to 10000 Å and is deposited by thin film techniques such as evaporation or sputtering to compose a three-layer structure. Parallel strips of back electrodes 5 made of Al are disposed on the laminate opposed to and in a direction orthogonal to the transparent electrodes 2.

Such a thin film EL element has the EL substance 4 sandwiched between the inductive substances 3a, 3b, and it may be regarded as a capacitive element from the viewpoint of equivalent circuit. This thin film EL element is driven by applying a relatively high voltage of about 200 V across the electrodes and its voltage-brightness curve is shown in FIG. 2. This thin film EL element emits light at high brightness by AC electric field, and has a long life.

The basic display drive of the thin film EL display apparatus using such a thin film EL element as a display panel is achieved by applying a writing voltage sequentially to the scanning side electrodes and a modulation voltage corresponding to the display data to determine emission and non-emission to the data side electrodes. Either one of transparent electrodes 2 and back electrodes 5 of the thin film EL element can be used as scanning side electrodes or data side electrodes. The superposing effect or cancelling effect of the writing voltage and modulating voltage occurs at the intersecting pixel area of the scanning side electrode and data side electrode of the EL layer. A voltage greater than the emission start voltage or less than the emission start voltage is applied across the electrodes, and each pixel is set in an emission state or non-emission state, so that a desired display is obtained.

A conventional method for driving such a thin film EL display to obtain a gradated display, is to vary the brightness of each pixel by applying a modulation voltage to each pixel corresponding to the level of brightness desired. The modulation

voltage is applied to the data electrodes and corresponds to gradation display data supplied to the display drivers.

FIG. 3 is a circuit diagram showing a part of the output of the data side driver circuit of a thin film EL display apparatus which is driven utilising the voltage modulation method outlined above, in order to obtain a gradated display. FIG. 4 is a timing chart showing the operation of the circuit. In FIG. 3, an input terminal 6 receives a ramp waveform voltage V_{RA} as shown in FIG. 4(1), and is connected to one of the terminals of a capacitor 8 through a switch 7. The other terminal of the capacitor 8 is grounded. The connecting point of the switch 7 and capacitor 8 is connected to each gate of an N-channel MOS transistor 9 and a P-channel MOS transistor 10.

The drain of the N-channel MOS transistor 9 is connected to a power supply 11 for supplying a voltage V_{VCC} corresponding to the maximum modulation voltage applied to the data side electrode. The source of the transistor 9 is connected to the source of the P-channel MOS transistor 10, and the drain of transistor 10 is grounded. The connecting point of the source of N-channel MOS transistor 9 and the source of the P-channel MOS transistor 10 is connected to an output terminal 12.

In such a data side drive circuit, when a ramp waveform voltage V_{RA} shown in FIG. 4(1) begins to be applied to the input terminal 6, the switch 7 is turned on. The ON duration of the switch 7 is set according to the gradation display data mentioned above. When the switch 7 is turned on, an electric current flows into the capacitor 8, and the capacitor 8 is charged to a voltage depending upon how long the switch 7 is ON (from time t_0 to t_1 in FIG. 4), i.e., the gradation display data. This charging voltage is applied to the gates of the respective transistors 9, 10, and the N-channel MOS transistor 9 is turned on, and the P-channel MOS transistor 10 is turned off. The output terminal 12 delivers an output voltage as shown in FIG. 4(3), corresponding to the charging voltage of the capacitor 8, which is the modulation voltage V_m corresponding to the gradation display data. This modulation voltage V_m is applied to the data side electrode, and by varying this modulation voltage V_m , the brightness of the corresponding pixel can be varied and gradation display is effected.

In this drive method, however, the N-channel MOS transistor 9 is not always turned on in a saturated state, and the ON resistance varies with the voltage applied to the gate, i.e. the gradation display data. This ON resistance can be a high value. The thin film EL element is a large-sized capacitive display element, and the quantity of current flowing per channel (a circuit for one pixel) in the drive circuit is large, and thus the heat loss

at the N-channel MOS transistor 9 can become very significant if the ON resistance is high. It is hence difficult to integrate such transistors when composing a drive circuit in an integrated circuit. Additionally, in the manufacturing process of such an integrated circuit, since the P-channel MOS transistor and N-channel MOS transistor of high voltage resistance must be assembled, the manufacturing cost of integrated circuit is very high, which has made it hard to realize practically.

Also, in such thin film EL display apparatus, a method of driving a gradated display known as the pulse width modulation method has been used. In this method the brightness of pixels is varied by varying the pulse width of the modulation voltage in accordance with gradation display data.

In this drive method, however, the gradation brightness is not stable as explained below, and many stages of gradation cannot be set.

FIG. 5(1), (2), (3) show applied voltage waveforms to pixels in a supposed pulse width modulation method, the waveform of the power supply current at this time, and the waveform of the current flowing in the emission layer of the pixels.

As shown in FIG. 5(1), the effective voltage V_A applied to a pixel is the superposed value of the modulation voltage V_M applied to the data side electrode, and the writing voltage V_W applied to the scanning side electrode having a reverse polarity to the modulation voltage V_M , and in a magnitude corresponding to the emission threshold voltage V_{th} . When the effective voltage V_A of such a rectangular wave is applied to a pixel, the waveform of the power supply current is as shown in FIG. 5(2).

That is, while the effective voltage V_A is below the emission threshold voltage V_{th} , a nearly constant current which does not contribute to the emission current flows in the capacitive portion of the pixel. When the effective voltage V_A exceeds the emission threshold voltage V_{th} , the current flowing in the emission layer is as shown in FIG. 5(3). The current portion flowing in the emission layer of the pixel, that is the current portion contributing to emission, is added to the current portion flowing in the capacitive component of the pixel, as shown in FIG. 5(2). The emission brightness of pixels is proportional to the current quantity of the current flowing in the emission layer.

Here, when the pulse width of the modulation voltage V_M is limited as indicated by broken line in FIG. 5(1), the current flowing in the emission layer is shut off at the fall point of the modulation voltage V_M . That is, by limiting the pulse width of the modulation voltage V_M , the quantity of current flowing in the emission layer of pixel is controlled, so that a brightness corresponding to the pulse width of the modulation voltage V_M is obtained.

However, when the effective voltage V_A applied to pixels is a rectangular wave, that is, when the modulation voltage V_M is a rectangular wave, the current flowing in the emission layer is a peak current, and its duration is short (as indicated by t_l in FIG. 5(1)). Thus, it is difficult to set the pulse width of the modulation voltage V_M in multiple stages, which means it is impossible to control the brightness of the pixels in multiple stages. Additionally, at each brightness level the current flowing in each emission layer is large, hence only a slight error in the pulse width of the modulation voltage V_M may result in a large change in the brightness, this makes it difficult to stabilize the gradation of brightness.

In this drive method, for example, when transparent electrodes of high line resistance are used as data side electrode, the modulation voltage applied to the data side electrodes is affected by the line resistance, and a brightness difference occurs among pixels as described below.

FIG. 6 is a connection diagram of a display panel 13 of thin film EL display apparatus and part of its drive circuit, presented to explain the cause of such brightness difference. In FIG. 6, the data side electrodes 14a, 14b are connected to output ports 15a, 15b of a data side drive circuit for applying modulation voltage V_M to these data side electrodes 14a, 14b. A plurality of scanning side electrodes 16a, 16b, 16c, 16d are disposed mutually parallel in a direction orthogonal to the data side electrodes 14a, 14b, and these scanning side electrodes 16a to 16d are respectively connected to output ports 17a, 17b, 17c, 17d of a scanning side drive circuit for applying writing voltage $-V_W$ to them. In FIG. 6, intermediate line resistances of the data side electrodes 14a, 14b are indicated by resistance R .

In such a thin film EL display if two pixels 18A and 18D are to be displayed at the same brightness then a writing voltage $-V_W$ is sequentially applied to scanning side electrodes 16a and 16d, and the same modulation voltage V_M is sequentially applied to the data side electrode 14a. Thus, the brightness of each pixel 18A and 18D should be identical.

Pixel or picture element 18A is located at a position near output port 15a. Since the line length of the data side electrode 14a from output port 15a to pixel 18A is short, the effect of the line resistance is almost negligible. Therefore a voltage having nearly the same waveform as the modulation voltage V_M delivered from the output port 15A is applied to the pixel 18A, as shown in FIG. 7(1). At this time, when a writing voltage $-V_W$ having the waveform shown in FIG. 7(2) is applied from the output port 17a of the scanning side drive circuit to the scanning side electrode 16a, an effective volt-

age having the waveform as shown in FIG. 7(3) is applied to pixel 18A.

In contrast, pixel 18D is remote from output port 15a, and the length of the data side electrode 14a from the output port 15a to the pixel 18D is long and thus the line resistance R in this length is large, and the modulation voltage V_M is greatly affected by the line resistance R. Therefore, a voltage waveform as shown in FIG. 8(1) is applied to the pixel 18D. Such a waveform is as if the modulation voltage is being driven into an integrating circuit. At this time, when a writing voltage $-V_W$ having the waveform as shown in FIG. 8(2) is applied from the output port 17d of the scanning side drive circuit to the scanning side electrode 16d, an effective voltage having the form as shown in FIG. 8(3) is applied to the pixel 18D.

With respect to the effective voltages applied to the pixels 18A, 18D, the voltage substantially contributing to emission is the portion over the emission threshold voltage V_{th} . When the waveform in FIG. 7(3) and the waveform in FIG. 8(3) are compared with respect to the portion over the emission threshold voltage V_{th} , it is clear that the waveform in FIG. 8(3) is wider in area by the shaded area portion. This difference results directly in a difference in the brightness between pixels 18A and 18D. Even though it was intended that they emit the same brightness, the pixel 18D is actually brighter than the pixel 18A.

That is, if a modulation voltage V_M of identical waveform is applied to two separate pixels, the pixel closer to the output port is darker than the one furthest away, and the brightness fluctuates. If this difference in the brightness occurs between pixels vertically adjacent which should be identical in gradation, the display quality deteriorates.

Further examples of conventional methods of driving capacitive display devices are given in UK Patent Application GB 2,165,078A, and European Patent Applications EP 0,106,550 A3 and EP 0,187,347 A2.

It is an object of the present invention to alleviate the foregoing problems.

According to a first aspect of the invention, there is provided a method of driving a capacitive display device comprising a capacitive display layer interposed between a plurality of scanning electrodes and a plurality of data electrodes, said scanning electrodes and said data electrodes being arranged in mutually intersecting directions, said method comprising:

sequentially applying writing pulses to said scanning electrodes; and

applying data pulses, which are pulse width modulated in accordance with gradation display data to said data electrodes;

said data pulses and said writing pulses being

such that their combined respective voltage magnitudes are greater than a minimum voltage necessary for emitting light from said display device, characterised in that said data pulses have a voltage magnitude which increases continuously during the period of each of said data pulses.

According to a second aspect of the invention, there is provided apparatus for driving a capacitive display device comprising:

a capacitive display layer interposed between a plurality of scanning electrodes and a plurality of data electrodes, said scanning electrodes and said data electrodes being arranged in mutually intersecting directions;

scanning electrode driving means for sequentially applying writing pulses to said scanning electrodes; and

data electrode driving means for applying data pulses pulse width modulated in accordance with gradation display data to said data electrodes in order that a potential difference between said scanning electrodes and said data electrodes activates said capacitive display layer, characterised by means for causing said data pulses to have a voltage magnitude which increases continuously during the period of each of said data pulses.

An advantage of the above-defined method and apparatus is that a ramp voltage can be applied to the data electrodes as a modulation voltage, and therefore the peak value of the current flowing in the emission layer of pixels as the current contributing to the emission can be kept low, and the current passing time is extended. Thus, the pulse width of the modulation voltage may be set in multiple stages, and the current flowing in the emission layer becomes smaller at each stage of brightness, and the gradation of brightness is stabilized.

According to a third aspect of the invention there is provided apparatus for driving a capacitive display device comprising:

a pair of mutually opposed electrodes having a capacitive display layer interposed therebetween; and

a D.C. power supply, characterised in that there is provided an impedance converting means disposed electrically in series between said D.C. power supply and one of said electrodes and having an impedance which varies in accordance with a control signal applied thereto; and

a control signal generating means for generating said control signal and applying said control signal to said impedance converting means; and

switching means being provided for causing a current to be applied from said impedance converting means to said one of said electrodes under the control of said control signal for a time period according to the gradation display data.

An advantage of this latter arrangement is that the drive device capable of displaying in gradations can be made at low cost by simplifying the manufacturing process and keeping heat loss of transistors in the device low.

In preferred embodiments the impedance converting means and/or the switching means is composed of N-channel MOS transistors.

In one embodiment the control signal generating means is adapted to generate the control signals so as to vary in amplitude over the time period.

In this embodiment the control signals increase in voltage level over the time period, the impedance of the impedance converting means decreasing for an increase in the voltage amplitude of the control signal.

In another embodiment, the impedance converting means comprises a transistor arranged to switch from an ON state to an OFF state upon inversion of said control signal thereby to terminate said time period of current application, and wherein the resulting pulse width modulated data pulse output from said transistor does not change in voltage over the pulse width.

An advantage of this arrangement is that since the modulation pulse applied to the data electrodes for gradation display does not change in voltage, while only the pulse width is varied in accordance with the gradation display data, the aforesaid transistor in the driving circuit for delivering the modulation pulse may be always turned on in its saturated state, and the heat loss of the transistor may be kept low and the drive circuit may be easily fabricated in the integrated circuit. Furthermore, since the high withstand voltage transistor in the integrated circuit is composed of N-channel MOS alone, the cost of the integrated circuit may be reduced.

Some preferred embodiments of the invention will now be described by way of example with reference to Figures 9 to 24 of the accompanying drawings. In the drawings:-

FIG. 1 is a partially cut-away perspective view of a thin film EL element, FIG. 2 is a graph showing the voltage-brightness characteristic of thin film EL element, FIG. 3 is a circuit diagram showing one output part of data side drive circuit of thin film EL display apparatus to which a conventional drive method is applied, FIG. 4 is a timing chart showing its operation, FIG. 5(1), (2), (3) are waveform diagrams showing the voltage applied to pixels, power source current, and current flowing in emission layer of pixels in the conventional drive method, respectively, FIG. 6 is a circuit diagram showing an outline structure of essential parts of a thin film EL display apparatus to which a conventional drive method is

applied, FIG. 7 is a waveform diagram showing the voltage applied to pixels positioned on scanning side electrode near output port of the same thin film EL display apparatus, FIG. 8 is a waveform diagram showing a voltage applied to pixels on the scanning electrode remote from the output port of the same thin film EL display apparatus, FIG. 9 is a block diagram showing an outline structure of thin film EL display apparatus to which a drive method as one of the embodiments of this invention is applied, FIG. 10 is a circuit diagram showing one output part of the same data side drive circuit, FIG. 11 is a timing chart showing its operation, FIG. 12 is a graph showing the relation between pulse width and brightness, FIG. 13 is a block diagram showing an outline structure of its ramp voltage generating circuit, FIG. 14 is a circuit diagram showing a practical composition of this ramp voltage generating circuit, FIG. 15 (1), (2), (3) are waveform diagrams showing the voltage applied to the pixels, power source current, and current flowing in the emission layer of the pixels, respectively, FIG. 16 is a block diagram showing an outline structure of a thin film EL display apparatus to which a drive method as other embodiment of this invention is applied, FIG. 17 is a timing chart showing its basic operation, FIG. 18 is a block diagram showing an outline structure of a correcting circuit for correcting the brightness of this thin film EL display apparatus, FIG. 19 is a timing chart showing the operation of this correcting circuit, FIG. 20 is a waveform diagram showing the voltage applied to the pixels positioned on the first scanning side electrode of the same thin film EL display apparatus, FIG. 21 is a waveform diagram showing the voltage applied to the pixels positioned on the m-th scanning side electrode of the thin film EL display apparatus, FIG. 22 is a block diagram showing an outline structure of a thin film EL display apparatus to which a drive method of an embodiment of the invention is applied, FIG. 23 is a block diagram showing an outline structure of a correcting circuit for correcting the brightness of the same thin film EL display apparatus, and FIG. 24 is a timing chart showing the operation of this correcting circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 9 is a block diagram showing an outline structure of a thin film EL display device 21 as a capacitive display device to which a drive method as one of the embodiments of the invention is applied. In the drawing, a display panel 22 is made

of thin film EL element, and its practical composition is same as explained in the prior art, and the same explanation is omitted here. Scanning side electrodes Y1, Y2, ..., Yn (collectively indicated by reference code Y) of the display panel 22 are connected to a scanning side drive circuit 24, and data side electrodes X1, X2, ..., Xn (collectively indicated by reference code X) of the display panel 22 are connected to a data side drive circuit 26, and a display control circuit 27 for controlling these circuits is connected to the scanning side drive circuit 24 and data side drive circuit 26.

FIG. 10 is a circuit diagram showing an outline structure of the output portion corresponding to an arbitrary pixel of the data side drive circuit 26. In FIG. 10, a counter 28 is a circuit for counting clocks ϕ for gradation given from the display control circuit 27, and it is connected to a comparator 29. A latch circuit 30 is a circuit for holding the gradation display data given from the display control circuit 27 while illuminating the corresponding pixel, and it is also connected to the comparator 29. Here, as the gradation display data per pixel, 4-bit data "D0, D1, D2, D3" is given, and the gradation of 16 stages is obtained.

The comparator 29 possesses a function for delivering a voltage V_A at H level when the counting of the counter 28 coincides with the gradation display data "D0, D1, D2, D3" held by the latch circuit 30. The comparator 29 is connected to the gate of a first N-channel MOS transistor 32 through an inverter 31, and is also connected to the gate of a second N-channel MOS transistor 33. The drain of the first N-channel MOS transistor 32 is connected to a power supply 34 for feeding a potential HVCC of the modulation pulse, and the source of this first transistor 32 is connected to the drain of the second N-channel MOS transistor 33, and the source of the second transistor 33 is grounded.

The connecting point of the source of the first N-channel MOS transistor 32 and the drain of the second N-channel MOS transistor 33 is connected to an output terminal 35. Between the source and gate of the first N-channel MOS transistor 32, a zener diode 36 for passing a current in a reverse direction to the transistor 32 is connected.

FIG. 11 is a timing chart showing the operation of the gradation display drive by the above thin film EL display apparatus 21, and FIG. 12 is a graph showing the relation between the pulse width and brightness of the modulation pulse applied to an EL substance 4 (see FIG. 1). This EL substance 4 possesses a characteristic to increase the brightness when the applied voltage is higher, or when the applied time is longer if the voltage is constant. On the basis of this characteristic, it is possible to control to display the EL substance 4 in gradation by the PWM system.

When a binary code of, for example, "0111" is applied from the display control circuit 27 to the latch circuit 30 as gradation display data "D3, D2, D1, D0," if clocks ϕ for gradation are sequentially entered from the display control circuit 27 into the counter 28 as shown in FIG. 11 (1), the counting of the counter 28 first becomes "0000" by the first clock ϕ input, and the counting increases at every input of clock ϕ thereafter.

When eight clocks ϕ for gradation are entered in the counter 28, and its counting reaches the gradation display data "D3, D2, D1, D0" held by the latch circuit 30, the output voltage V_A of the comparator 29 is inverted from L level to H level as shown in FIG. 11 (2). As a result, the gate potential of the first N-channel MOS transistor 32 and the gate potential of the second N-channel MOS transistor 33 are respectively changed from the hitherto H level to L level and L level to H level, and the first transistor 32 is inverted from ON to OFF, and the second transistor 33 is inverted from OFF to ON. Therefore, the modulation voltage V_m taken out from the output terminal 35 is inverted from H level to L level when eight clocks ϕ for gradation are entered into the counter 28.

Up to this point of inversion, a voltage equal to the voltage HVCC of the power supply 34 is being applied to the gate of the first N-channel MOS transistor 32, and the H level of the voltage of the output terminal 35 when the first transistor 32 is turned on, that is, the modulation voltage V_m , is nearly equal to the voltage HVCC of the power supply 34.

Meanwhile, the time width of the waveform of this modulation voltage V_m possessing a frequency of 1 MHz to 500 kHz, or the pulse width of modulation pulse, varies along with the gradation display data shown above, and the pulse width is broadened as the value of the gradation display data increases. This modulation voltage V_m is applied to the data side electrodes 25 containing one pixel corresponding to it.

At this time, the scanning side electrodes Y are provided with a writing voltage V_w equal to the threshold voltage V_{th} at which the voltage level starts light emission of the EL layer in the reverse polarity to the modulation voltage V_m . Therefore, the above pixel is provided with an active voltage in the waveform as shown in FIG. 11 (5) on the basis of the scanning side electrode Y, and the pixel emits light only for the period of pulse width of the modulation pulse.

That is, the emission brightness of the pixel varies depending on the gradation display data, and gradation display is effected. Incidentally, application of writing pulse into the scanning side electrodes Y is effected in linear sequence of the scanning side electrodes Y, and accordingly the

gradation display data is sequentially changed into the data corresponding to the pixels contained in the corresponding scanning side electrodes Y. Furthermore, in the above driving operation, in the first field, when a writing pulse of negative polarity with respect to, for example, the data side electrodes X is applied to the scanning side electrodes Y, in the second field, a writing pulse of positive polarity with respect to the scanning side electrodes Y is applied to the data side electrodes X, so that AC driving for repeating the first field and second field alternately is effected.

In the case of the above driving, the drain and source are nearly at the same potential when the first N-channel MOS transistor 32 is turned on, and the heat loss caused by the flowing current is kept low.

FIG. 13 is a block diagram showing an outline structure of a ramp voltage generating circuit 37 for supplying a ramp voltage at modulation voltage V_M to the output stage of the data side drive circuit 26. In FIG. 13, a constant current circuit 38 is a circuit for passing a specific current by receiving a modulation start signal V_{M-ON} from other functional part of the data side drive circuit 26, and it is connected to the power supply HVCC and also to one of the terminals of the capacitor 39, while the other terminal of the capacitor 39 is grounded.

A converter 40 is a circuit for receiving a charging voltage of a capacitor 39, and delivering a voltage V_R varying according to this charging voltage, and it is connected to the power supply HVCC and also to the connecting point A of the constant current circuit 38 and capacitor 39. Between the connecting point A and the ground, a switch 41 to be turned on by receiving a modulation end signal V_{M-OFF} given from other functional part of the data side drive circuit 26 is connected. The voltage of the power supply HVCC is set at the peak value of the modulation voltage V_M .

FIG. 14 is a circuit diagram showing an example of practical composition of a ramp voltage generating circuit 37 shown in FIG. 13. In FIG. 14, the constant current circuit 38 is composed of resistances R1, R2, R3, N-channel MOS transistor Q1, and PNP transistor Q2.

That is, resistances R1, R2 are connected in series, and one end of the resistance R1 is connected to the power supply HVCC, and the other end of the resistance R2 is connected to the drain of the N-channel MOS transistor Q1, and the source of this transistor Q1 is grounded, and a voltage of H level is applied to the gate of this transistor Q1 as modulation start signal V_{M-ON} . At the connecting point B of the resistances R1, R2, the base of the PNP transistor Q2 is connected, and the emitter of the transistor Q2 is connected to the power supply HVCC through resistance R3,

and the collector of the transistor Q2 is connected to one of the terminals of the capacitor 13.

The converter 40 is composed of N-channel MOS transistor Q3, and the gate of the transistor Q3 is connected to the connecting point A of the capacitor 39 and transistor Q2, and the drain of the transistor Q3 is connected to the power supply HVCC, and the source of the transistor Q3 is connected to the output stage of the data side drive circuit 26 shown above (FIG. 9).

The transistor Q3 has a sufficient current supply capacity, and its source voltage does not vary depending on the output stage of the data side drive circuit 26. The switch 41 is composed also of N-channel MOS transistor Q4, and its drain is connected to the connecting point A, and its source is grounded, and a voltage of H level is applied to its gate as modulation termination signal V_{M-OFF} .

FIG. 15 (1), (2), (3) show the applied voltage waveform to the pixel in the gradation display driving in the thin film EL display apparatus 21 described above, the waveform of the supply current at this time, and the waveform of the current flowing in the emission layer of the pixel, respectively. Referring to these waveform diagrams, the operation is described below.

From time t_0 , application of writing voltage V_w from the scanning side drive circuit 24 shown in FIG. 9 to the scanning side electrodes Y is started, and when the writing voltage V_w reaches the emission threshold voltage V_{th} (time t_1), H level voltage is applied to the gate of the transistor Q1 of the ramp voltage generating circuit shown in FIG. 14 as modulation start signal V_{M-ON} . As a result, the transistor Q1 is turned on, and the base potential of the transistor Q2 is lowered, and the transistor Q2 is turned on. Sequentially, a constant current begins to flow from the power supply HVCC into the capacitor 39 through resistance R3 and transistor Q2.

The charging voltage of the capacitor 39 rises at a specific gradient as the time passes. Therefore, in the transistor Q3 which receives this charging voltage as gate signal, its output or the source voltage V_R increases in proportion to the charging voltage. That is, the output of the transistor Q3 becomes a ramp voltage V_R elevating at a specific gradient with the passing of the time. This ramp voltage V_R is supplied to the output stage of the data side drive circuit 26, and is applied to the data side electrodes X as modulation voltage V_M .

After a specific time T (time t_3), H level voltage applied to the gate of the transistor Q4 of the ramp voltage generating circuit 37 shown in FIG. 14 as modulation termination signal V_{M-OFF} , and the electric charge in the capacitor 39 is discharged, and the charging voltage in the capacitor 39 is suddenly lowered, and the ramp voltage V_R drops

at the same time. In this way, the modulation voltage V_M in the ramp waveform with pulse width T is applied from the data side drive circuit 26 into the data side electrodes X .

At this time, the effective voltage V_A applied to the corresponding pixel becomes a waveform as indicated by solid line in FIG. 15 (1). Therefore, the waveform of the power supply current at this time becomes as shown in FIG. 15 (2), that is, the passing time after the effective voltage V_A has exceeded the emission threshold voltage V_{th} becomes longer. Meanwhile, the effective voltage V_A is not rectangular wave, but is a superposed wave of the rectangular writing voltage V_w and modulation voltage V_M of ramp waveform, and therefore, the power supply current is not a peak current but attenuates smoothly.

This tendency directly continues in the current flowing in the emission layer of the pixel, and the waveform of this current is kept low in the peak value as shown in FIG. 15 (3), and attenuates smoothly to becomes a waveform having a long passing time. Besides, by setting the pulse width of the modulation voltage V_M making up the ramp waveform in several short steps as indicated by single dot chain line 11 in FIG. 15 (1), the current passing time flowing in the emission layer of the pixel shown in FIG. 15 (2) can be also shortened, and gradation display is realized.

In this case, since the current passing time flowing in the emission layer of the pixel is longer than in the prior art, the variably setting range of the pulse width of modulation voltage V_M , that is, the effective movable range indicated by symbol t in FIG. 15 (1) is widened, and the gradation display of multiple stages can be easily effected.

Moreover, the peak value of the current flowing in the emission layer of the pixels can be kept low, and the current at the brightness of each gradation stage is small, and the brightness does not change significantly due to error in the pulse width of the modulation voltage V_M , so that the gradation of each stage can be stably displayed.

In this embodiment, it is explained to drive the thin film EL display apparatus 21, but this invention may be similarly applied to driving of other capacitive display apparatus such as plasma display.

FIG. 16 is a block diagram showing an outline structure of a thin film EL display apparatus 21a to which a drive method of other embodiment of the invention is applied. In the drawing, a display panel 22 is made of thin film EL element, and its practical composition is same as the structure explained in the prior art, and the same explanation is omitted here. Plural scanning side electrodes $Y_1, Y_2, \dots, Y_{m-1}, Y_m$ arranged on the display panel 22 are connected to a scanning side drive circuit 24 disposed at the right side of FIG. 16. In a direction

orthogonal to the scanning side electrodes Y_1 to Y_m , plural data side electrodes $X_1, X_2, \dots, X_{n-1}, X_n$ are connected to a data side drive circuit 26 disposed in the upper side of FIG. 16.

In the scanning side drive circuit 24, output circuits 42 are individually connected to the scanning side electrodes Y_1 to Y_m , and through these output circuits 42, writing voltage $-V_w$ or $+V_w$ is selectively applied to the scanning side electrodes Y_1 to Y_m from a minus power supply 43A to which a switch 58A is connected or from a plus power supply 43B to which a switch 58B is connected. These output circuits 42 are connected to a shift register 44, and in synchronism with a clock CLK3 entered from the clock input terminal of the shift register 44, scanning data S-DATA for setting the scanning side electrodes Y_1 to Y_m in linear sequence is transferred to the shift register 44, so that the output circuits 42 are turned on in the linear sequence of the scanning side electrodes Y_1 to Y_m .

On the other hand, in the data side driving circuit 26, output circuits 45 which are switches for push-pull action being composed of C-MOS transistors are individually connected to the data side electrodes X_1 to X_n , and through these output circuits 45, the modulation voltage V_M is selectively applied to the data side electrodes X_1 to X_n from a power supply 46 having a switch 49. Besides, depending on the setting state of the output circuit 45, the data side electrodes X_1 to X_2 are clamped to the ground.

These output circuits 45 are connected to a comparator 47. This comparator 47 is connected to shift register 49 by way of a latch circuit 48. The shift register 49 makes a shift action in synchronism with the clock CLK1 entered from the clock input terminal, and transfers the gradation display data corresponding to the data side electrodes X_1 to X_n , and the data transferred to the shift register 49 is sent to the comparator 47.

The comparator 47 possesses a function for determining the gradation width corresponding to the gradation display data, by comparing the 3-bit parallel data sent from the counter 50 with the gradation display data given from the latch circuit 48. In FIG.16, meanwhile, each pixel in the display panel 22 is equivalently expressed by capacitors.

FIG. 18 is a block diagram showing a correcting circuit 51 for correcting the brightness difference among pixels caused by the line resistance of data side electrodes X_1 to X_n . In the correcting circuit 51 in FIG. 18, the clock generator 52 is a circuit for generating a fundamental clock CLK for determining the gradation width corresponding to the gradation display data, and it can be operated by the enable signal CLKE given from its input terminal.

In the next stage of the clock generator 52, a delay circuit 53 is connected which delays the fundamental clock CLK by a predetermined amount and applies it as clock CLK2 of the counter 50 in the data side drive circuit 26. A scanning line position detection circuit 54 is connected to this delay circuit 53. The scanning line position detection circuit 54 possesses the functions for counting up and counting down the horizontal sync signals HD entered from the input terminal 55 as clocks, and it is reset by a vertical sync signal VD entered from the input terminal 56.

The count-up signal or count-down signal of the scanning line position detection circuit 54 is sent into the delay circuit 53, and delay is processed in the delay circuit 53 according to the quantity corresponding to this signal. At the input terminal 57 of the scanning line position detection circuit 54, a signal EDD for determining which one of the above count-up signal or count-down signal should be sent into the delay circuit 53 is entered. In this embodiment, the signal EDD is set at L level, and a count-down signal is sent to the delay circuit 53. When the signal EDD is set at H level, meanwhile, a count-up signal is sent into the delay circuit 53.

The basic operation of the thin film EL display apparatus 21a in FIG. 16 is explained below while referring to the timing chart shown in FIG. 17.

To the shift register 49 of the data side drive circuit 26, gradation display data is transferred in a form of 3-bit binary code in synchronism with the clock CLK1. This 3-bit gradation display data is temporarily held in the latch circuit 48. In this state, the clear signal CLR hitherto entered in the comparator 47 and counter 50 is canceled as shown in FIG. 17 (1) (time t1), the data side electrode X corresponding to the data of "0" out of the gradation display data held in the latch circuit 48 is clamped to the ground level, and all other data side electrodes X corresponding to other data are pulled up to the modulation voltage V_M .

Suppose, for example, gradation display data 0, 2, 4, and 7 are given to the output ports 45 corresponding to the data side electrodes X1, X2, Xn-1, Xn of the data side drive circuit 26. At this time, the output circuit 45 of the data side electrode X1 is clamped to the ground simultaneously with cancellation of clear signal \overline{CLR} , thereby becoming the waveform shown in FIG. 17 (3). That is, the gradation width is set at zero.

At the output circuit 45 of the data side electrode X2, on the other hand, the counting of the clocks CLK2 [see FIG. 17 (2)] counted by the counter 50 is compared with the gradation display data "2" in the comparator 47, and this counting value clamped to the ground level at the timing of becoming "2" (time t2), and the gradation width Tw

of the waveform shown in FIG. 17 (4) is set. Likewise, the output circuit 45 of the data side electrode Xn-1 is clamped to the ground level at the timing when the counting of the counter 50 becomes 4 (time t3), and the gradation width T4 of the waveform shown in FIG. 17 (5) is set. As for the output circuit 45 of the data side electrode Xn, similarly, it is clamped to the ground level at the timing (time t4) when the counting of the counter 50 becomes 7, and the gradation width T7 of the waveform shown in FIG. 17 (6) is set. Therefore, at the data side electrodes X1, X2, Xn-1, Xn, modulation voltages V_M in the pulse width corresponding to the gradation display data 0, 2, 4, 7 are applied.

On the other hand, in the scanning side drive circuit 24, while the clear signal CLR is being canceled by the data side drive circuit 26, one of all output circuits 42 is turned on, and the writing voltage $-V_w$ is applied only to one corresponding scanning side electrode Y. In the next field, the writing voltage $+V_w$ is applied in the same way.

When the above operation is repeated in the linear sequence of the scanning side electrodes Y, the pixels positioned on each scanning electrodes Y emit light or do not, depending on the gradation display data, and a screen having gradation in brightness is displayed on the whole.

Next is explained the operation of brightness correction by the correcting circuit 51 shown in FIG. 18 by referring to the timing chart shown in FIG. 19.

A clock generator 52 delivers a fundamental clock CLK in the waveform shown in FIG. 19 (1) as the basis for determining the gradation width. In the scanning line position detection circuit 54, after being reset by receiving a vertical sync signal VD, the horizontal sync signals HD are counted down as clock. In this count-down action, the number "m" of the horizontal sync signal HD in one field is set as the initial value. When the first horizontal sync signal HD in the field is counted, the count-down signal "m-1" is sent into the delay circuit 53. At the delay circuit 53, by the portion corresponding to this count-down signal "m-1" delay processing is conducted on the fundamental clock CLK as shown in FIG. 19 (2), and this clock is given to as clock CLK2 of the counter 50 of the data side drive circuit 26.

In this case, since the count-down signal "m-1" is large, the delay amount Ta corresponding to the fundamental clock CLK of the clock CLK2 is large. Therefore, in the data side drive circuit 26, the timing for starting counting of the clock CLK2 in the counter 50 is significantly delayed, and a modulation voltage V_M of pulse width $t_A + T_a$ larger than the pulse width t_A corresponding to the gradation data by the portion of delay amount Ta is applied.

FIG. 20 shows the waveform of applied voltage to the pixel A at the intersecting position between the first scanning side electrode Y1 and the data side electrode X1. Specifically, FIG. 20 (1) shows the waveform of modulation voltage V_M applied from the data side electrode X1, and FIG. 20 (2) shows the waveform of the writing voltage $-V_w$ corresponding to the emission threshold voltage V_{th} given from the first scanning side electrode Y1. The effective voltage applied to the pixel A at this time has the waveform as shown in FIG. 20 (3).

That is, at this pixel A, since a modulation voltage V_M with a pulse width of $t_A + T_a$ wider by the delay portion T_a of the clock CLK2 than the pulse width t_A corresponding to the gradation display data as explained above is applied, the area is increased by the portion indicated by the shaded area in FIG. 20 (3) of the portion higher than the emission threshold voltage V_{th} contributing to the emission at the effective voltage, so that it is corrected to a higher brightness by the portion of this area increase.

In the correcting circuit 51 in FIG. 18, when the count-down of the scanning line position detection circuit 54 is advanced, when the count-down signal becomes m-m or zero, the delay amount in the delay circuit 53 becomes zero, and the delay amount with respect to the fundamental clock CLK of the clock CLK2 becomes also zero. Therefore, at the data side drive circuit 26, the starting timing for counting the clock CLK2 in the counter 50 is not delayed, and the modulation voltage V_M in the pulse width t_A corresponding to the gradation display data is applied. In this case, since the count-down signal of the scanning line position detection circuit 54 is m-m, writing voltage $-V_w$ is applied to the scanning side electrode Y_m .

FIG. 21 shows the waveform of the applied voltage to the pixel B at the intersecting position with the data side electrode X1, same as the above case of the m-th scanning side electrode Y_m shown above. Specifically, FIG. 21 (1) shows the integration distribution when the modulation voltage V_M applied from the data side electrode X1 is influenced by the line resistance of transparent electrode, and FIG. 21 (2) denotes the waveform of writing voltage $-V_w$ corresponding to the emission threshold voltage V_{th} given from the m-th scanning side electrode Y_m . Therefore, at this time, the effective voltage applied to the pixel B becomes the waveform as shown in FIG. 21 (3).

In this case, since the pixel B is remote from the output circuit 45, it is much influenced by the line resistance, and the applied modulation voltage V_M becomes an integration waveform as shown in FIG. 21 (1), and of the portion over the emission threshold voltage V_{th} contributing to emission at the effective voltage, the shaded area in FIG. 21 (3)

is increased.

However, if the same gradation display data as the pixel A positioned on the first scanning side electrode Y1 is set in the pixel B, the area increment indicated by shaded area in FIG. 20 (3) caused at the effective voltage in the case of pixel A when a modulation voltage V_M with a pulse width of $t_A + T_a$ greater than the pulse width t_A corresponding to the gradation display data mentioned above becomes nearly equal to the area increment due to the effect of the line resistance in the shaded area in FIG. 21 (3) at the effective voltage applied to the pixel B. In other words, between the pixels, A, B positioned on the same data side electrode X1, the brightness is identical for the same gradation display data.

The amount of correction of brightness is determined depending on the value of the count-down signal of the scanning line position detection circuit 54, and since the value of the count-down signal indicates the position of the scanning side electrode Y at which the writing voltage $-V_w$ is applied at that time. At last, therefore, by the portion of increase of line resistance, the amount of brightness correction decreases in the linear sequence of the scanning side electrodes Y, and the sum of the increment of brightness due to effects of line resistance and the increment of brightness due to brightness correction is always the same.

In this way, a same brightness is always obtained for the same gradation display data, between pixels over the entire screen.

In this embodiment, as shown in FIGS. 20 and 21, since the application timing of the modulation voltage V_M is set so that the rising part of the modulation voltage V_M may be dislocated from the portion corresponding to emission of the effective voltage applied to pixels, if the modulation voltage V_M is influenced by the line resistance to become integration waveform, that rising part does not matter particularly. On the other hand, when setting the application timing of the modulation voltage V_M so that the descending portion of the modulation voltage V_M may be dislocated from the portion contributing to emission of the effective voltage, the descending portion of the integration waveform does not matter, but the rising portion matters. This rising portion of the integration waveform acts to reduce the area of the effective voltage applied to the pixels as the effects of the line resistance becomes larger, reverse to the case of the foregoing embodiment, and in this case the brightness correction should be reverse to the embodiment. In other words, the signal EDD applied to the input terminal of the scanning line position detection circuit 54 shown in FIG. 18 should be set to H level, contrary to the case of the embodiment.

FIG. 22 is a block diagram showing an outline composition of thin film EL display apparatus 21b to which a drive method of a further different embodiment of the invention is applied. In the drawing, a display panel 22 is composed of thin film EL element, and its practical composition is same as explained about the prior art, and the same explanation is omitted here.

Plural scanning side electrodes Y1, Y2, ..., Ym-1, Ym arranged on the display panel 22 are connected to a scanning side drive circuit 24 disposed at the right side in FIG. 22. Of the plural data side electrodes X1, X2, ..., Xn-1, Xn arranged toward the orthogonal direction to the scanning side electrodes Y1 to Ym, odd-numbered data side electrodes X1, ..., Xn-1 (hereinafter arbitrary data side electrodes are indicated by symbol X) are connected to a first data side drive circuit 26a provided at the upper side in FIG. 22, and even-numbered data side electrodes X2, ..., Xn are connected to a second data side drive circuit 26b disposed at the lower side in FIG. 22.

In the scanning side driving circuit 24, output circuits 42 are individually connected to the scanning side electrodes Y1 to Ym, and writing voltage -Vw or voltage +Vw corresponding to the emission threshold voltage Vth is selectively applied to the scanning side electrodes Y1 to Ym from a minus power supply 43A or a plus power supply 43B through these output circuits 42. These output circuits 42 are connected to a shift register 44, and the scanning data S-DATA for setting the scanning side electrodes Y1 to Ym in linear sequence are transferred to the shift register 44 in synchronism with the clock CLK3 entered from the clock input terminal of the shift register 44, and the output circuits 42 are turned on in the linear sequence of the scanning side electrodes Y1 to Ym.

In the first data side drive circuit 26a, output circuits 45a are individually connected to odd-numbered data side electrodes X1, ..., Xn-1, and a modulation voltage Vm is selectively applied to the data side electrodes X1, ..., Xn-1 from the power supply 46 through these output circuit 45a. Besides, depending on the setting state of the output circuits 45a, the data side electrodes X1, ..., Xn-1 are clamped at the ground level.

These output circuits 45a are connected to a comparator 47a. The comparator 47a is connected to a shift register 49a through a latch circuit 48a. The shift register 49a is a circuit for transferring the gradation display data corresponding to the data side electrodes X1, ..., Xn-1 by shifting in synchronism with the clock CLK1 entered from the clock input terminal, and the gradation display data transferred to the shift register 49a is temporarily held in a latch circuit 48a, and is sent into the comparator 47a. The comparator 47a compares the 3-bit parallel

data given from the counter 50a and the gradation display data given from the latch circuit 48a, and determines the gradation width corresponding to the gradation display data.

The composition of the second data side drive circuit 26b is same as that of the first data side drive circuit 26a, and output circuits 45b are individually connected to the even-numbered data side electrodes X2, ..., Xn, and through these output circuits 45b, modulation voltage Vm is selectively applied to the data side electrodes X2, ..., Xn from the power supply 46.

These output circuits 45b are connected to a comparator 47b, and the comparator 47b is connected to a shift register 49b through a latch circuit 48b. The comparator 47b compares the 3-bit parallel data given from the counter 50b with the gradation display data given from the latch circuit 48b, and determines the gradation width corresponding to the gradation display data. In FIG. 22, meanwhile, the pixels in the display panel 22 are equivalently expressed by capacitors.

FIG. 23 is a block diagram showing a correcting circuit 51a for correcting the brightness difference among pixels caused due to the line resistance of the data side electrodes X1 to Xn in the above thin film EL display apparatus 21b. In the correcting circuit 51a in FIG. 23, a clock generator 52 is a circuit for generating a fundamental clock CLK for determining the gradation width corresponding to the gradation display data, and it is operated by an enable signal CLKE given from its input terminal.

At the next stage of the clock generator 52, a first delay circuit 53a for delaying the fundamental clock CLK by a predetermined amount and giving as a clock ODD-CLK2 of the counter 50a of the first data side drive circuit 26a, and a second delay circuit 53b for delaying the fundamental clock CLK by a predetermined amount and giving as a clock EVEN-CLK2 of the counter 50b of the second data side drive circuit 26b are connected. A scanning line position detection circuit 54 is connected to these delay circuits 53a, 53b.

This scanning line position detection circuit 54 has the function for counting up or down the horizontal sync signals HD entering from its input terminal 55 as clock, and it is reset by a vertical sync signal entering from the input terminal 56. Either the count-up signal or the count-down signal of the scanning line position detection circuit 54 is given to the first delay circuit 53a, and the other is given to the second delay circuit 53b, and delaying process is effected in the delay circuit 53a, 53b by the portion corresponding to these signals. A signal EDD for determining to send the count-up signal and count-down signal to either one of the two delay circuits 53a, 53b is fed into the input terminal

57 of the scanning line position detection circuit 54.

In this embodiment, the signal EDD is set at L level, and a count-down signal is given to the first delay circuit 53a, and a count-up signal is given to the second delay circuit 53b. When the signal EDD is set at H level, a count-up signal is given to the first delay circuit 53a, and a count-down signal is given to the second delay circuit 53b.

The basic operation of the thin film EL display apparatus 21b shown in FIG. 22 is explained below while referring to the timing chart shown in FIG. 17.

To the shift registers 49a, 49b of the first and second data side drive circuits 26a, 26b, gradation display data is transferred in a form of 3-bit binary code in synchronism with the clock CLK1. This 3-bit gradation display data is temporarily held in the latch circuits 48a, 48b. In this state, the clear signal $\overline{\text{CLR}}$ entered hitherto in the comparators 47a, 47b and counters 50a, 50b is cleared as shown in FIG. 17 (1), and then the data side electrode X corresponding to "0" data among the gradation display data held in the latch circuits 48a, 48b is clamped at the ground level, and all other data side electrodes X corresponding to the other data are pulled up to the modulation voltage V_M .

Suppose the gradation display data 0, 2, 4, and 7 are given to the output circuits 45a, 45b corresponding to the data side electrodes X1, X2, Xn-1, Xn of the data side drive circuit 26a, 26b. At this time, the output circuit 45a of the data side electrode X1 is clamped at the ground level simultaneously with clearing (time t0) of the clear signal $\overline{\text{CLR}}$ to become a waveform as shown in FIG. 17 (3). That is, the gradation width is set to zero.

At the output circuit 45b of the data side electrode, the counting value of the clock CLK2 counted by the counter 50b as shown in FIG. 17 (2) is compared with the gradation display data "2" in the comparator 47b, and when the counting becomes 2 (time t1), it is clamped at the ground level, and the gradation width T2 in the waveform shown in FIG. 17 (4) is set. Likewise, the output circuit 45a of the data side electrode Xn-1 is clamped at the ground level when the counting of the counter 50a becomes 4 (time t2), and the gradation width T4 in the waveform shown in FIG. 17 (5) is set. The output circuit 45b of the data side electrode Xn is clamped at the ground level when the counting of the counter 50b becomes 7 (time 3), and the gradation width T7 in the waveform shown in FIG. 17 (6) is set. Therefore, in the data side electrodes X1, X2, Xn-1, Xn, modulation voltages V_M in the pulse width corresponding to the gradation display data 0, 2, 4, and 7 are applied.

On the other hand, in the scanning side drive circuit 24, while the clear signal $\overline{\text{CLR}}$ is being canceled in the data side drive circuits 26a, 26b, only one of the output circuits 42 is turned on, and

a writing voltage $-V_w$ corresponding to the emission threshold voltage V_{th} is applied only one corresponding scanning side electrode Y.

When this operation is repeated in the linear sequence of the scanning side electrodes Y, the pixels on the scanning side electrodes Y are illuminated or not in the brightness corresponding to the gradation display data, and a screen having gradation in brightness on the whole is displayed.

The operation of the brightness correction by the correcting circuit 51a shown in FIG. 23 is described below by referring to the timing chart shown in FIG. 24.

The clock generator 52 delivers a fundamental clock CLK which becomes the basis for determining the gradation width [see FIG. 24 (1)]. In the scanning line position detection circuit 54, after being reset by receiving a vertical sync signal VD, the horizontal sync signals HD as clock are counted up and counted down at the same time. In the count-up operation, "0" is set as the initial value. In the count-down operation, the number "m" of the horizontal sync signals HD in one field is set as the initial value.

When the first horizontal sync signal VD is counted, this countdown signal "m-1" is sent into the first delay circuit 53a, and the count-up signal "1" is sent into the second delay circuit 53b. By the amount corresponding to the countdown signal "m-1" and the count-up signal "1" the delay circuits 53a, 53b delay the fundamental clocks CLK, and these clocks are given as clock ODD-CLK2 of the counter 50a of the first data side drive circuit 26a and clock EVEN-CLK2 of the counter 50b of the second data side drive circuit 26b.

In this case, since the countdown signal "m-1" is sufficiently larger than the count-up signal "1", the delay amount Ta of the clock ODD-CLK2 with respect to the fundamental clock CLK is sufficiently large as shown in FIG. 24 (3), while the delay amount Tb of the clock EVEN-CLK2 is a small value as shown in FIG. 24 (2). Therefore, in the first data side drive circuit 26a, the timing to start counting of the clock ODD-CLK2 in the counter 50a is considerably delayed, and a wider gradation than the gradation width corresponding to the gradation display data is set in the output circuit 45a, and a modulation voltage V_M of a wider pulse width tA-Ta than the pulse width tA corresponding to the gradation display data is applied to the odd-numbered data side electrodes X1, ..., Xn-1.

By contrast, in the second data side drive circuit 26b, the timing to start counting of the clock EVEN-CLK2 in the counter 50b is hardly delayed, and the gradation width nearly corresponding to the gradation display data is set in the output circuit 45b, and a modulation voltage V_M in a pulse width tA nearly corresponding to the gradation display

data is applied to the even-numbered data side electrodes X2, ..., Xn.

FIG. 20 shows the waveform of applied voltage corresponding to pixels at intersecting positions of the first scanning side electrode Y1 and odd-numbered data side electrodes X1, ..., Xn-1. Of them, FIG. 20 (1) indicates the waveform of modulation voltage V_M applied from the data side electrodes X1, ..., Xn-1, and FIG. 20 (2) shows the waveform of the writing voltage $-V_w$ corresponding to the emission threshold voltage V_{th} applied from the first scanning side electrode Y1.

The effective voltage applied to the above pixels at this time becomes as shown in FIG. 20 (3). That is, on these pixels, modulation voltage V_M in a pulse width $t_A + T_a$ wider than the pulse width t_A corresponding to the gradation display data by the portion of delay amount T_a of the clock ODD-CLK2 is applied as mentioned above, of the portion above the emission threshold voltage V_{th} contributing to emission at the effective voltage, the portion indicated by shaded area in FIG. 20 (3) is increased in the area, and the brightness is corrected to the higher side by the portion of this area increment.

On the other hand, FIG. 21 shows the waveform of applied voltage to pixels at the intersecting positions of the first scanning side electrode Y1 and the even-numbered data side electrodes X2, ..., Xn. Of them, FIG. 21 (1) indicates the waveform of the modulation voltage V_M applied from the data side electrodes X2, ..., Xn, and FIG. 21 (2) denotes the waveform of writing voltage $-V_w$ corresponding to the emission threshold voltage V_{th} applied from the first scanning side electrode Y1. Therefore, the effective voltage applied to the pixels at this time has the waveform as shown in FIG. 21 (3).

In this case, since the pixels are remote from the output circuit 45b, the effect of the line resistance is significant, and the modulation voltage V_M being applied becomes the integration waveform as shown in FIG. 21 (1), and of the portion above the emission threshold voltage V_{th} contributing to emission at the effective voltage, the portion indicated by shaded area in FIG. 21 (3) is increased.

Since the modulation voltage V_M in the pulse width t_A nearly corresponding to the gradation display data is applied to these pixels, if the same gradation display data are set in the odd-numbered data side electrodes X1, ..., Xn-1 and even-numbered data side electrodes X2, ..., Xn, the area increment indicated by shaded area in FIG. 20 (3) caused at the effective voltage applied to the pixels corresponding to the odd-numbered data side electrodes X1, ..., Xn-1 becomes nearly equal to the area increment due to the effect of line resistance indicated by shaded area in FIG. 21 (3) at the

effective voltage applied to the pixels corresponding to the even-numbered data side electrodes X2, ..., Xn. Therefore, among the pixels positioned on the first scanning side electrode Y1, the brightness is the same for same gradation display data.

In the correcting circuit 51a in FIG. 23, when the count-up or countdown of the scanning line position detection circuit 54 is advanced (therefore, the scanning side electrode Y to which the writing voltage $-V_w$ is applied is shifted downward at the same time), the delay amount T_a of the clock ODD-CLK2 delivered from the first delay circuit 53a is gradually decreased in response, while the delay amount T_b of the clock EVEN-CLK2 delivered from the second delay circuit 53b is gradually increased, and when the writing voltage $-V_w$ is applied to the middle scanning side electrode Y, the delay amounts T_a , T_b of the two clocks ODD-CLK2, EVEN-CLK2 become equal to each other.

At this time, at the pixel positioned on the middle scanning side electrode Y, the line length of the odd-numbered data side electrodes X1, ..., Xn-1 and the line length of the even-numbered data side electrodes X2, ..., Xn become equal to each other, and the effects of the line resistance are nearly identical. Accordingly, the brightness corrections of equivalent extents are effected, so that the brightness of pixels may be uniform.

When the count-up and count-down of the scanning line position detection circuit 54 in the correcting circuit 51a in FIG. 23 are further advanced (therefore, the scanning side electrode to which the writing voltage $-V_w$ is applied is shifted downward from the middle), the relation between the delay amount T_a of the clock ODD-CLK2 delivered from the first delay circuit 53a and the delay amount T_b of the clock EVEN-CLK2 delivered from the second delay circuit 53b is inverted, and the brightness correction corresponding to each delay amount is effected similarly on the corresponding pixels. In other words, the delay amounts T_a , T_b of two clocks ODD-CLK2, EVEN-CLK2 always keep a complementary relation within one field.

In this way, among the pixels in the entire screen, a same brightness is obtained for the same gradation display data.

In this embodiment, meanwhile, as shown in FIGS. 20 and 21, since the application timing of the modulation voltage V_M is set so that the rising part of the modulation voltage V_M may be dislocated from the portion contributing to the emission out of the effective voltage applied to the pixels, if the modulation voltage V_M is influenced by the line resistance to become integration waveform, its rising part does not pose any problem.

By contrast, when the application timing of the modulation voltage V_M is set so that the descending part of the modulation voltage V_M may be

dislocated from the portion contributing to the emission of the effective voltage, the descending part of the integration waveform does not matter, but the rising part poses a problem. The rising part of the integration waveform acts to decrease the area of the voltage applied to the pixels as the effect of the line resistance increases, reversely to the case of the above embodiment, and in this case the brightness should be corrected in the reverse manner of the shown embodiment. That is, the signal EDD applied to the input terminal of the scanning line position detection circuit 54 shown in FIG. 23 should be set to H level, contrary to the above embodiment.

Incidentally, this invention is not limited to the thin film EL display apparatus 21, 21a, 21b but it may be freely embodied in any arbitrary capacitive display apparatus such as plasma display apparatus.

Claims

1. A method of driving a capacitive display device (21) comprising a capacitive display layer interposed between a plurality of scanning electrodes (Y) and a plurality of data electrodes (X), said scanning electrodes (Y) and said data electrodes (X) being arranged in mutually intersecting directions, said method comprising:

sequentially applying writing pulses (Vw) to said scanning electrodes (Y); and

applying data pulses (Vm), which are pulse width modulated in accordance with gradation display data (D) to said data electrodes (X);

said data pulses (Vm) and said writing pulses (Vw) being such that their combined respective voltage magnitudes are greater than a minimum voltage necessary for emitting light from said display device (21), characterised in that said data pulses (Vm) have a voltage magnitude (V_R) which increases continuously during the period of each of said data pulses (Vm).

2. Apparatus for driving a capacitive display device (21) comprising:

a capacitive display layer interposed between a plurality of scanning electrodes (Y) and a plurality of data electrodes (X), said scanning electrodes (Y) and said data electrodes (X) being arranged in mutually intersecting directions;

scanning electrode driving means (24) for sequentially applying writing pulses (Vw) to said scanning electrodes; and

data electrode driving means (26) for applying data pulses pulse width modulated in

accordance with gradation display data to said data electrodes (X) in order that a potential difference between said scanning electrodes (Y) and said data electrodes (X) activates said capacitive display layer, characterised by means for causing said data pulses (Vm) to have a voltage magnitude (V_R) which increases continuously during the period of each of said data pulses (Vm).

3. Apparatus for driving a capacitive display device comprising:

a pair of mutually opposed electrodes (X,Y) having a capacitive display layer interposed therebetween; and

a D.C. power supply (34), characterised in that there is provided an impedance converting means (32; 40) disposed electrically in series between said D.C. power supply and one of said electrodes and having an impedance which varies in accordance with a control signal applied thereto; and

a control signal generating means (28 to 31; 38,39) for generating said control signal (V_A;A) and applying said control signal to said impedance converting means (32;40); and

switching means (29;38,41) being provided for causing a current to be applied from said impedance converting means to said one of said electrodes under the control of said control signal for a time period according to the gradation display data.

4. Apparatus according to claim 3, wherein the impedance converting means (32;40) and/or the switching means (29;38,41) comprise N-channel MOS transistors.

5. Apparatus according to claim 3 or claim 4, wherein said control signal generating means (38,39) is adapted to generate said control signal so as to vary in amplitude over said time period.

6. Apparatus according to claim 5, wherein said control signal generating means (38,39) is adapted to generate said control signal so as to increase in voltage level over said time-period, and wherein

the impedance of said impedance converting means (40) decreases for an increase in the voltage amplitude of said control signal.

7. Apparatus according to claim 3 or claim 4 wherein said impedance converting means comprises a transistor (32) arranged to switch from an ON state to an OFF state upon inversion of said control signal (VA) thereby to

terminate said time period of current application, and wherein the resulting pulse width modulated data pulse output from said transistor does not change in voltage over the pulse width.

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Fig.1 Prior Art

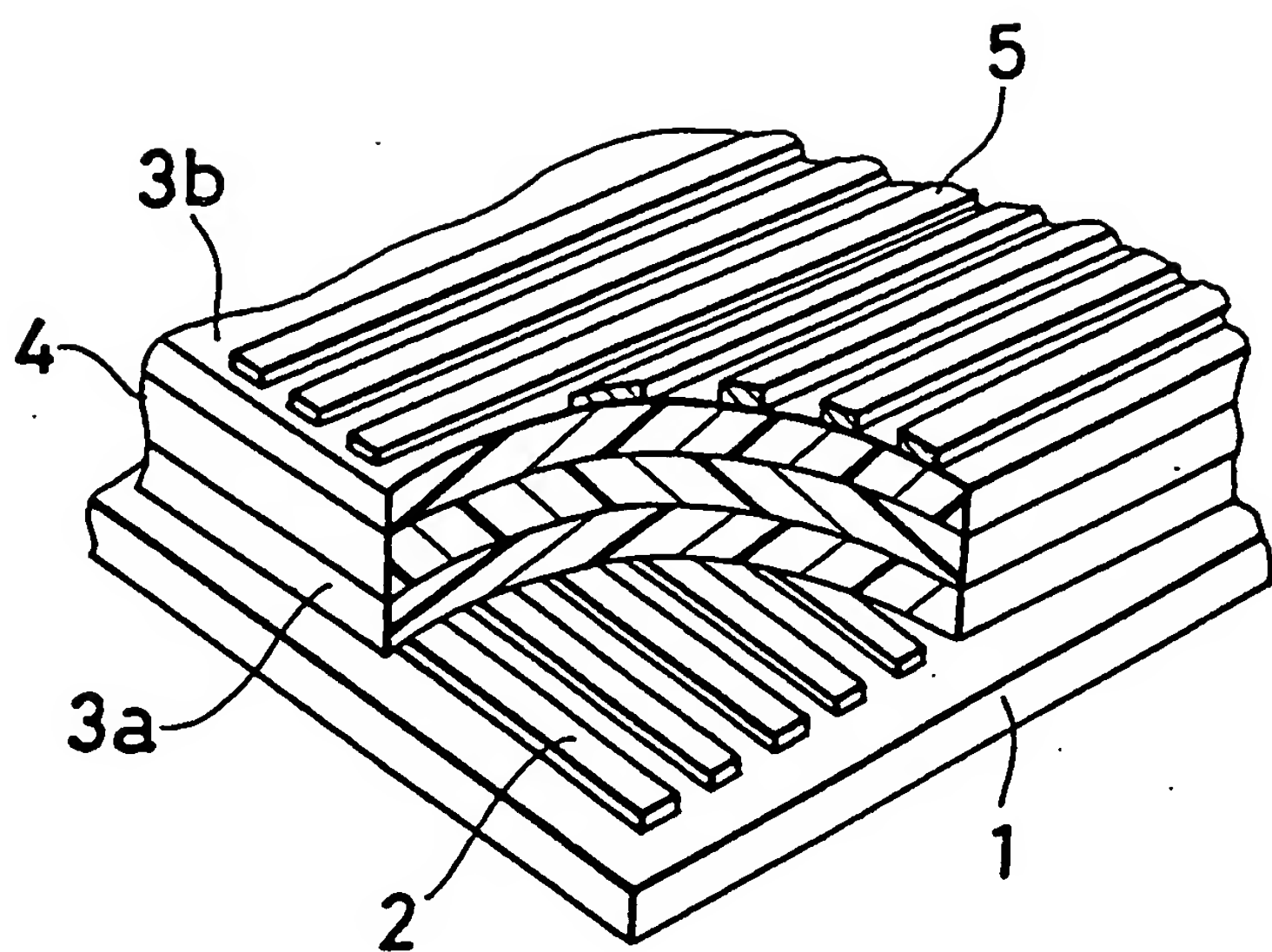


Fig.2 Prior Art

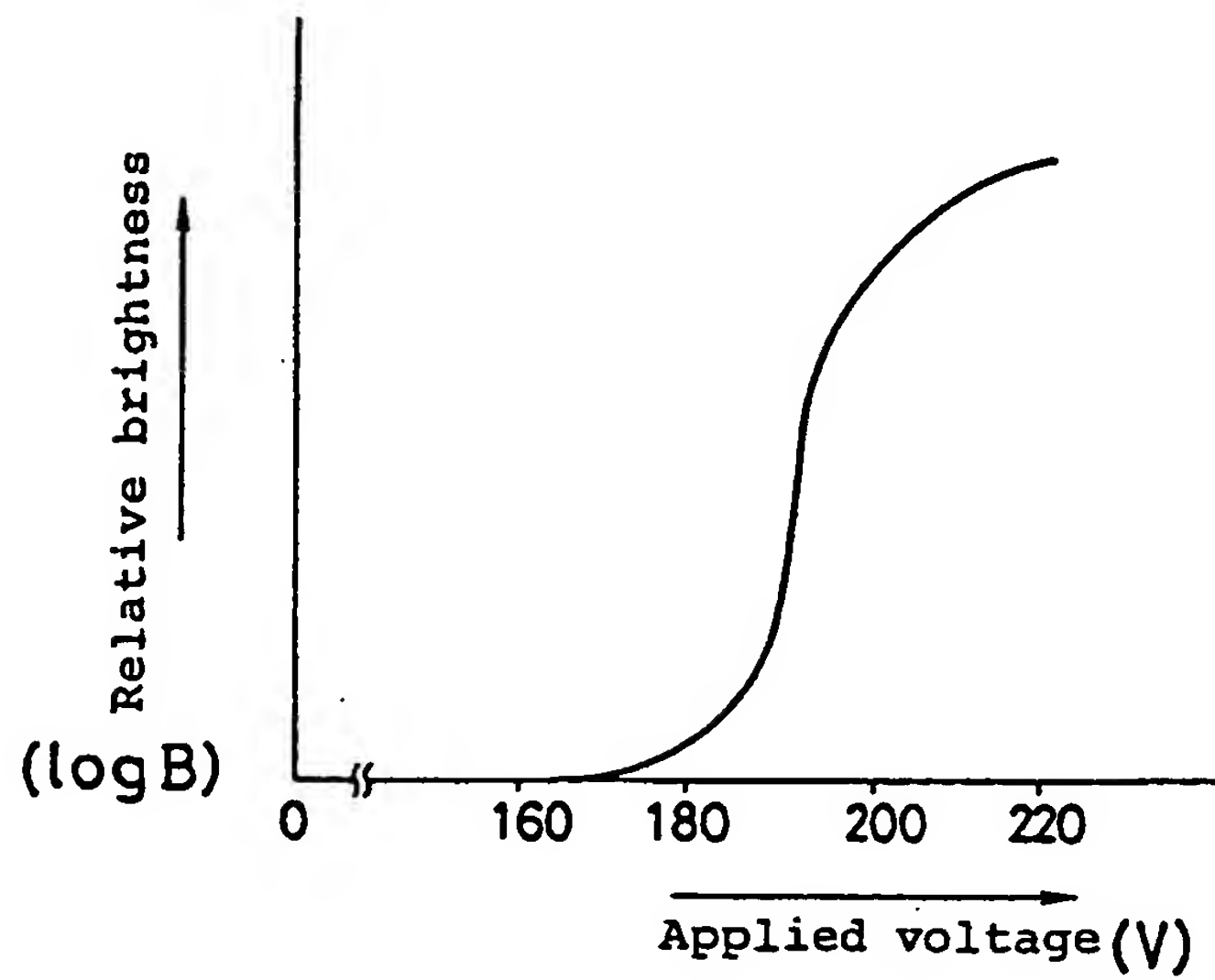


Fig.3 Prior Art

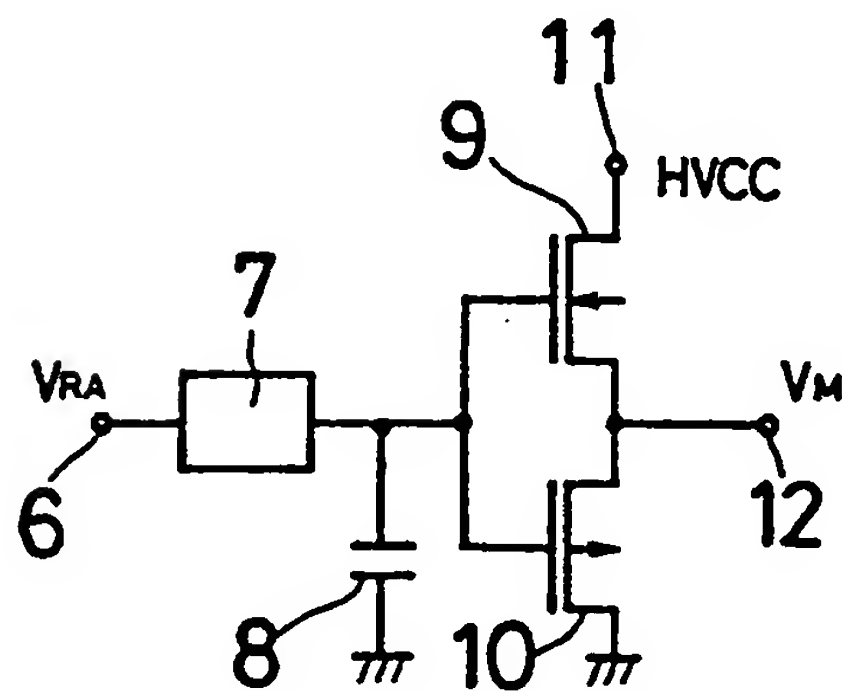


Fig.4 Prior Art

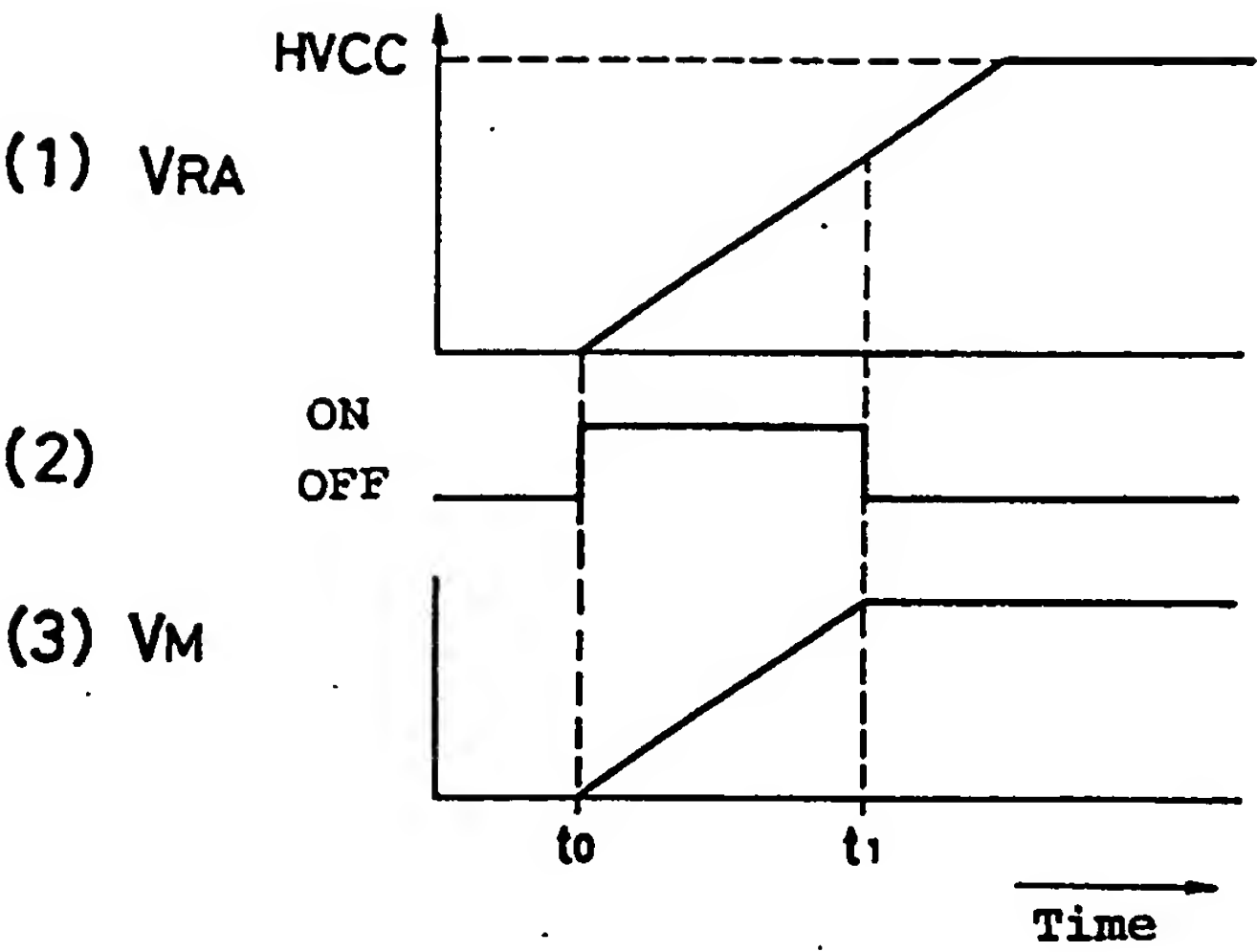


Fig.5 Prior Art

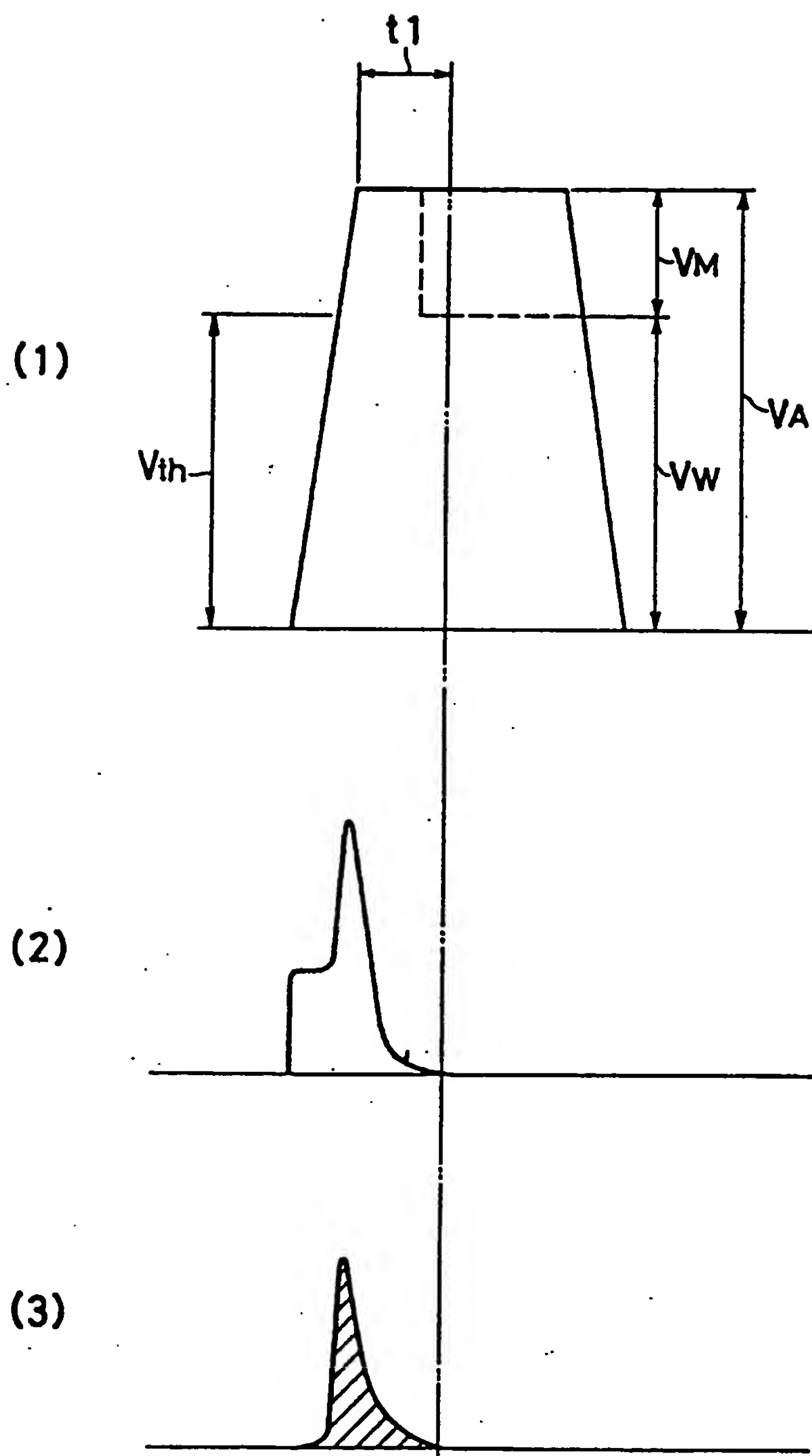


Fig.6 Prior Art

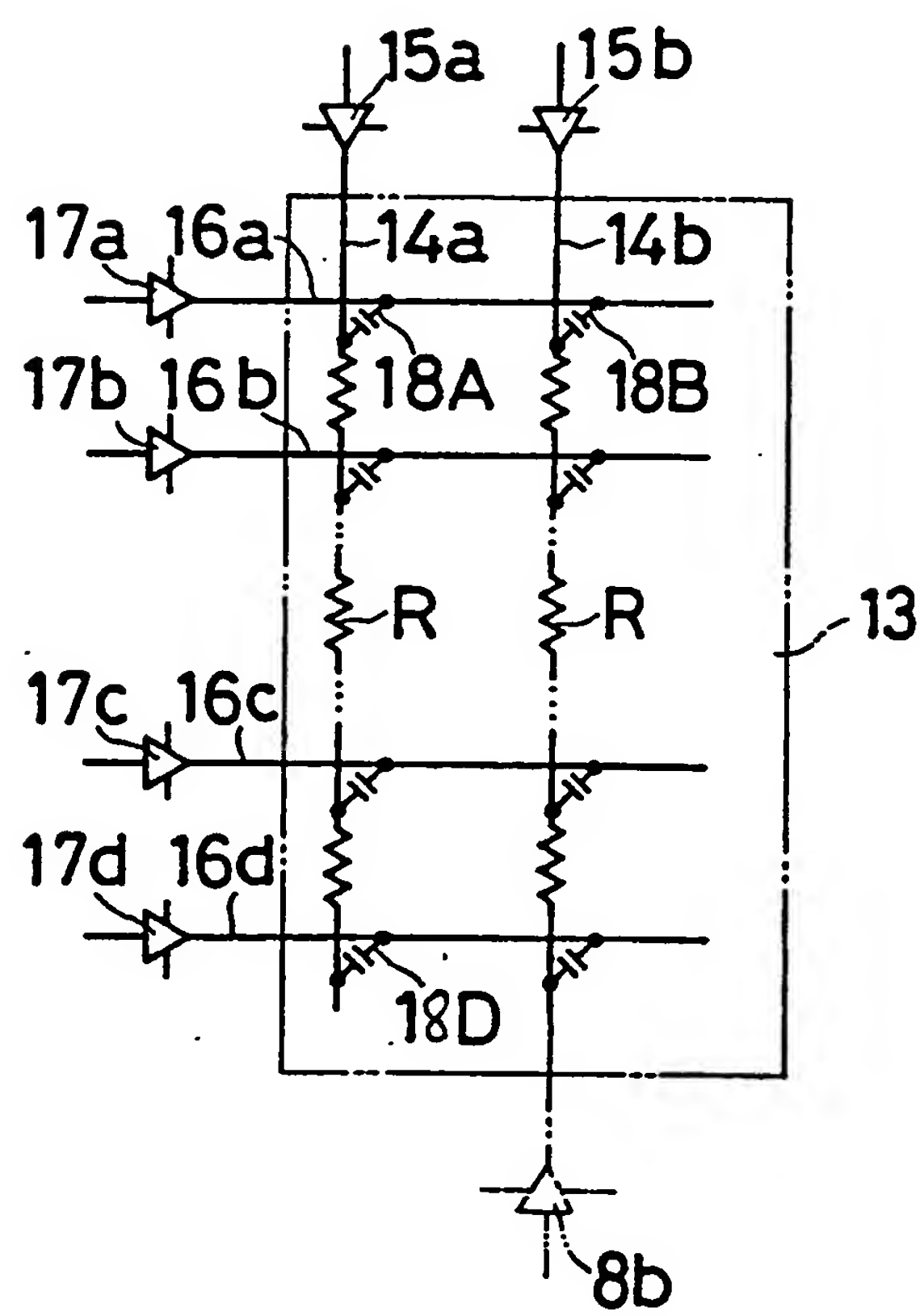


Fig. 7
Prior Art

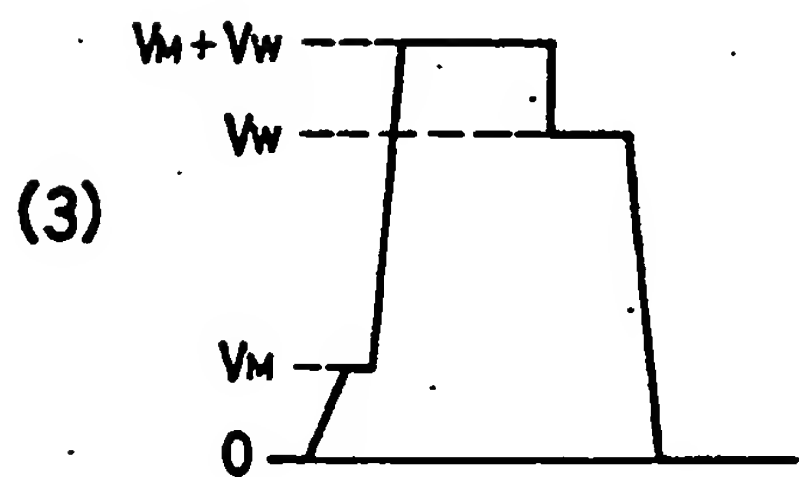
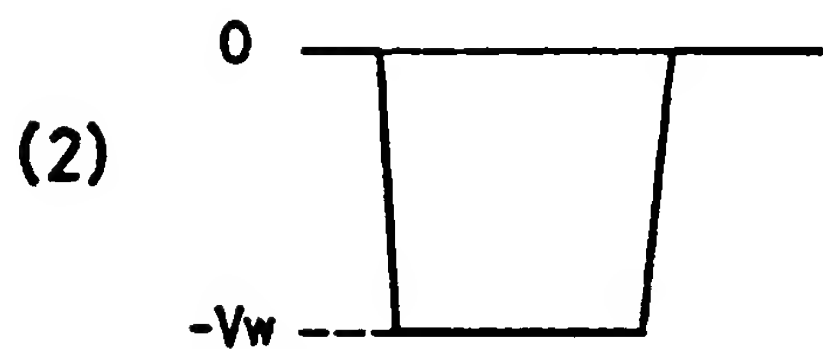


Fig. 8
Prior Art

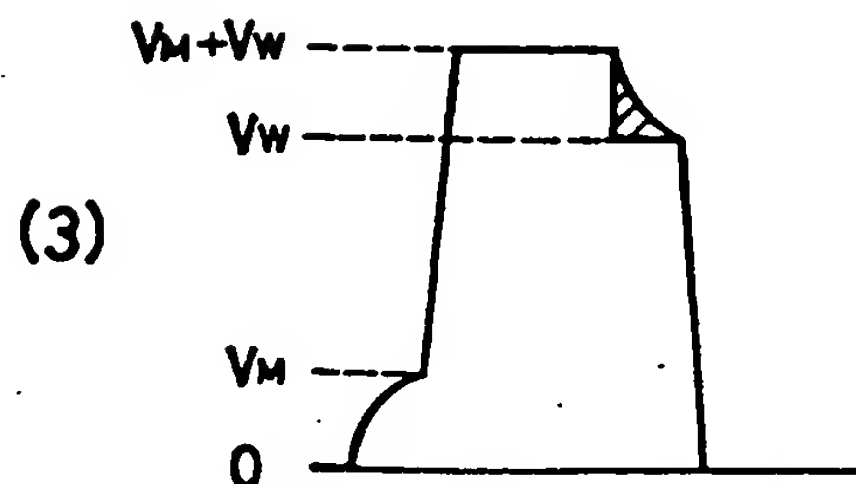
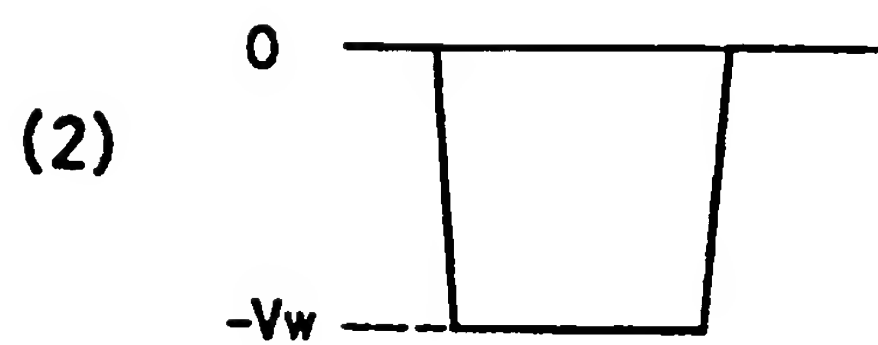
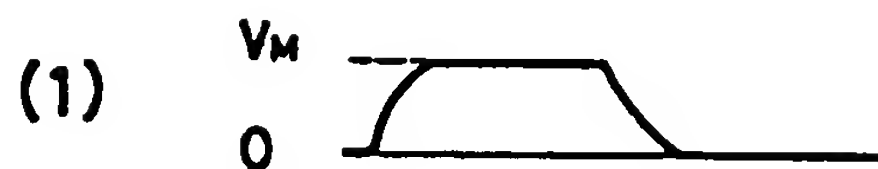


Fig.9

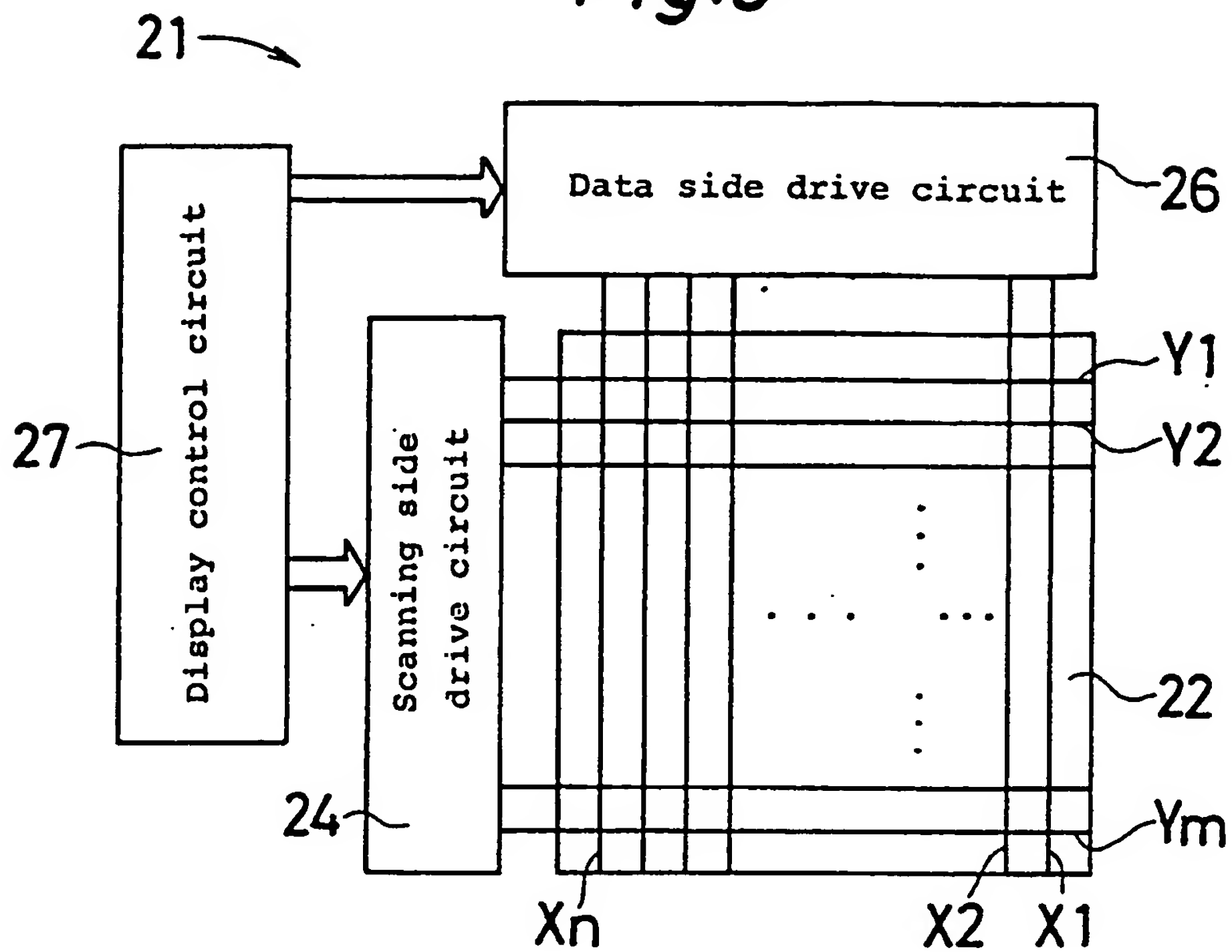


Fig.10

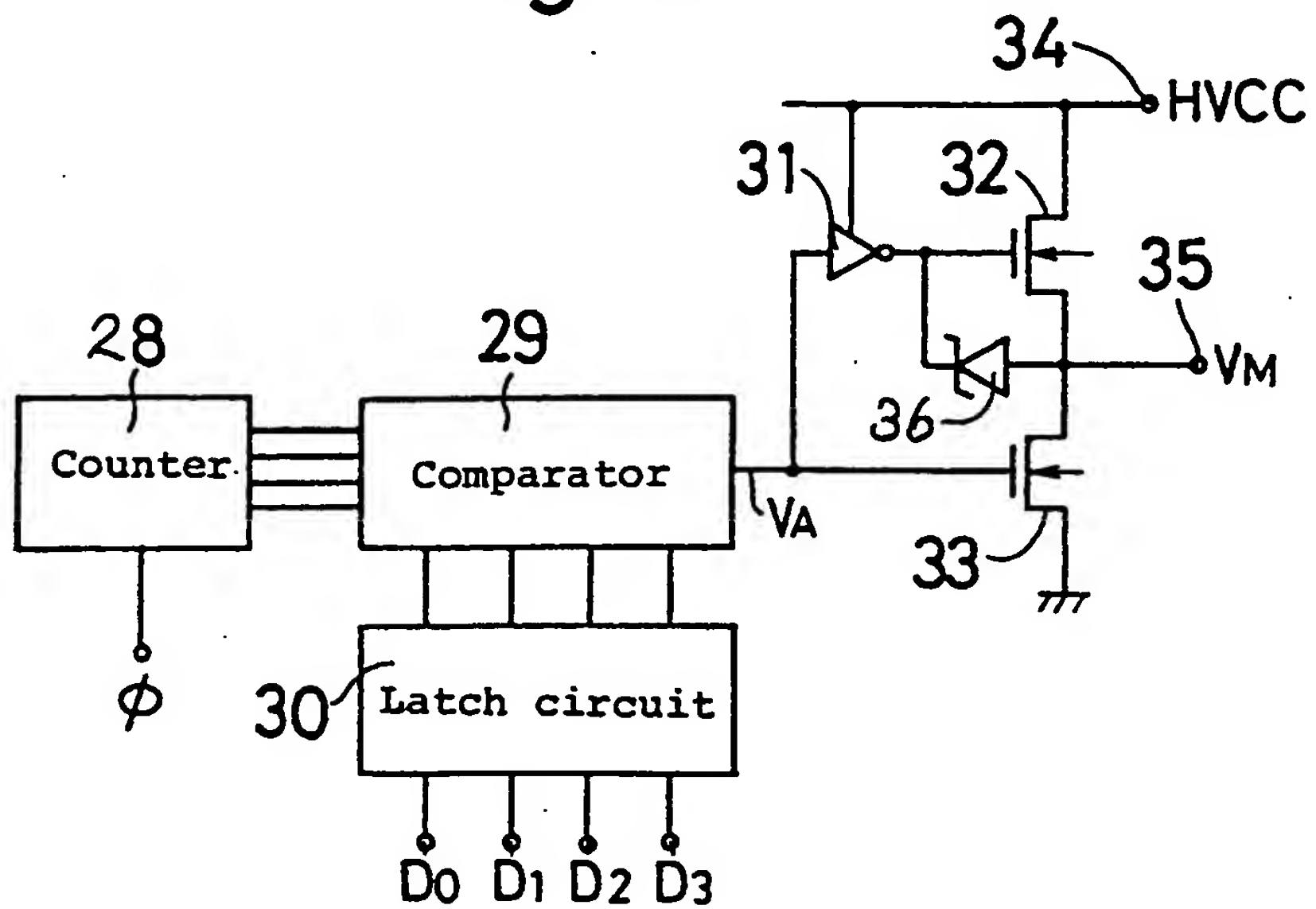


Fig.11

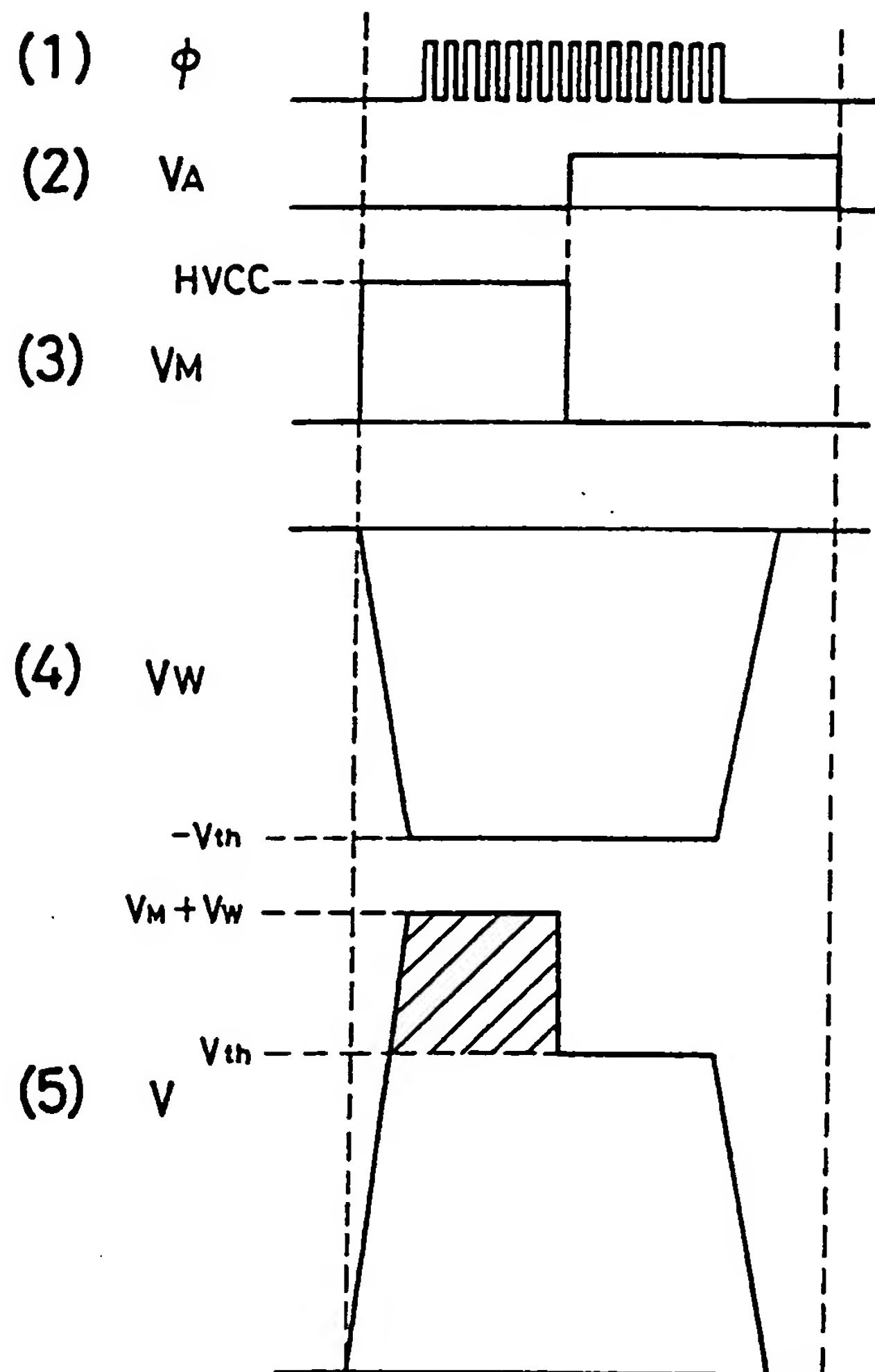


Fig.12

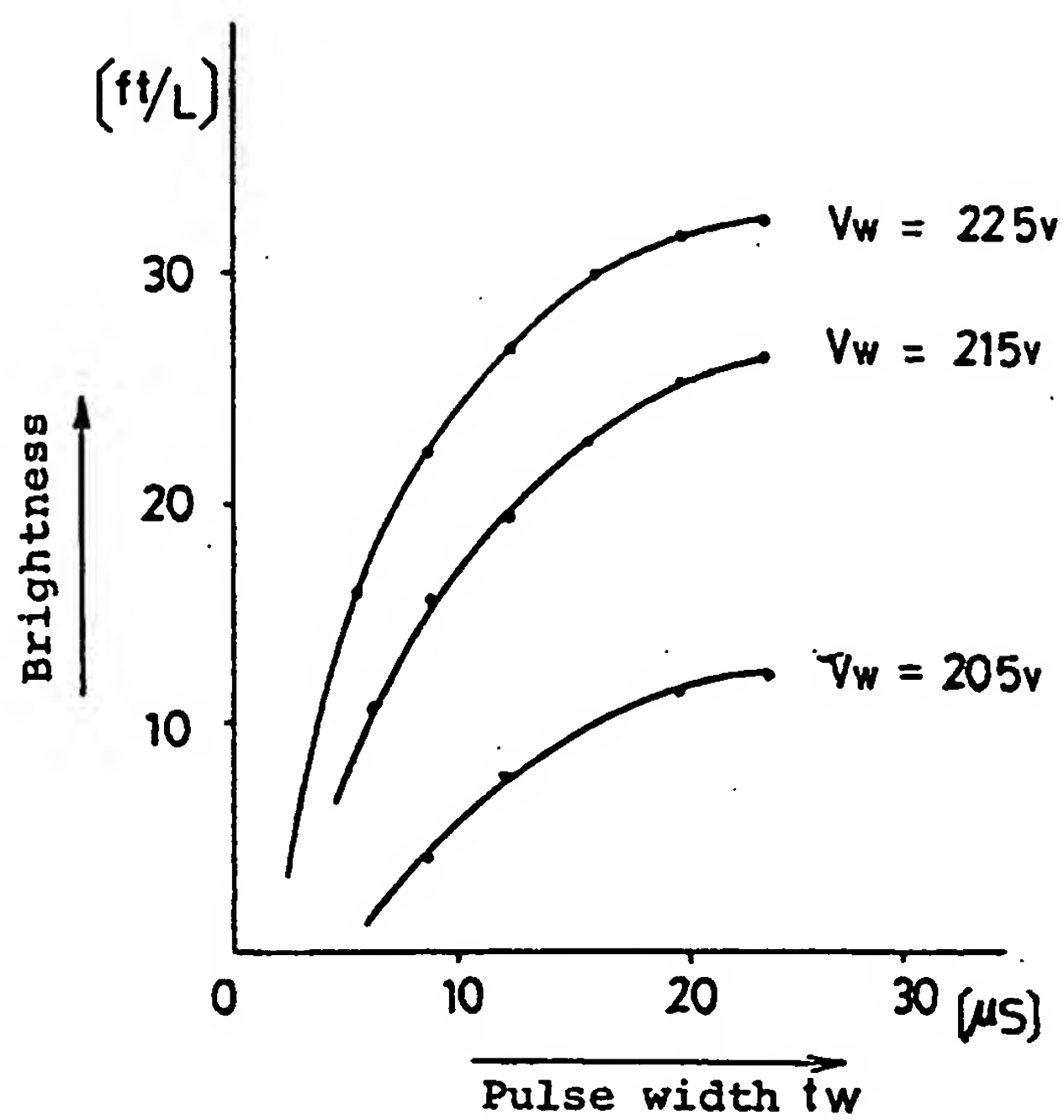


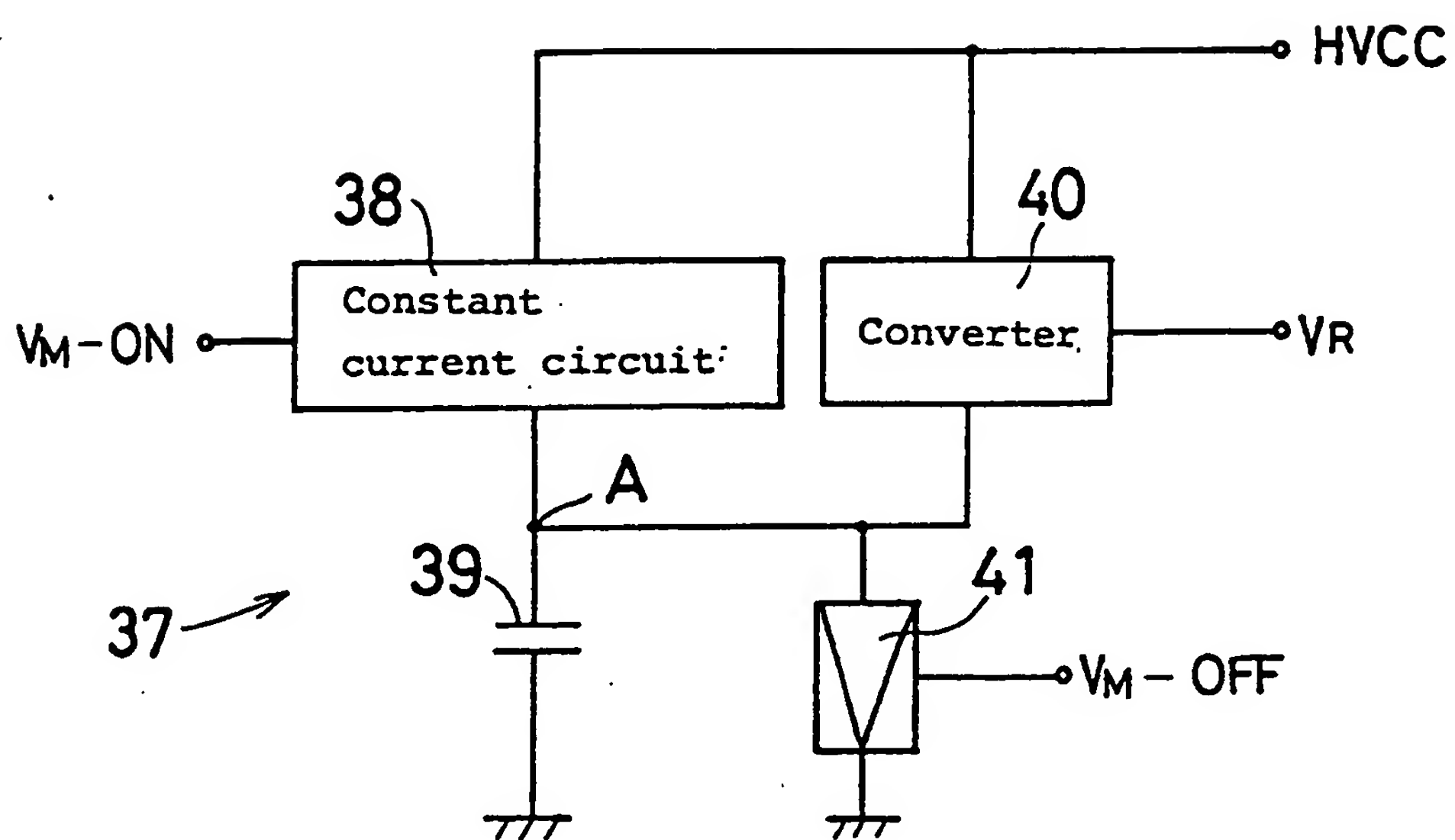
Fig.13

Fig.14

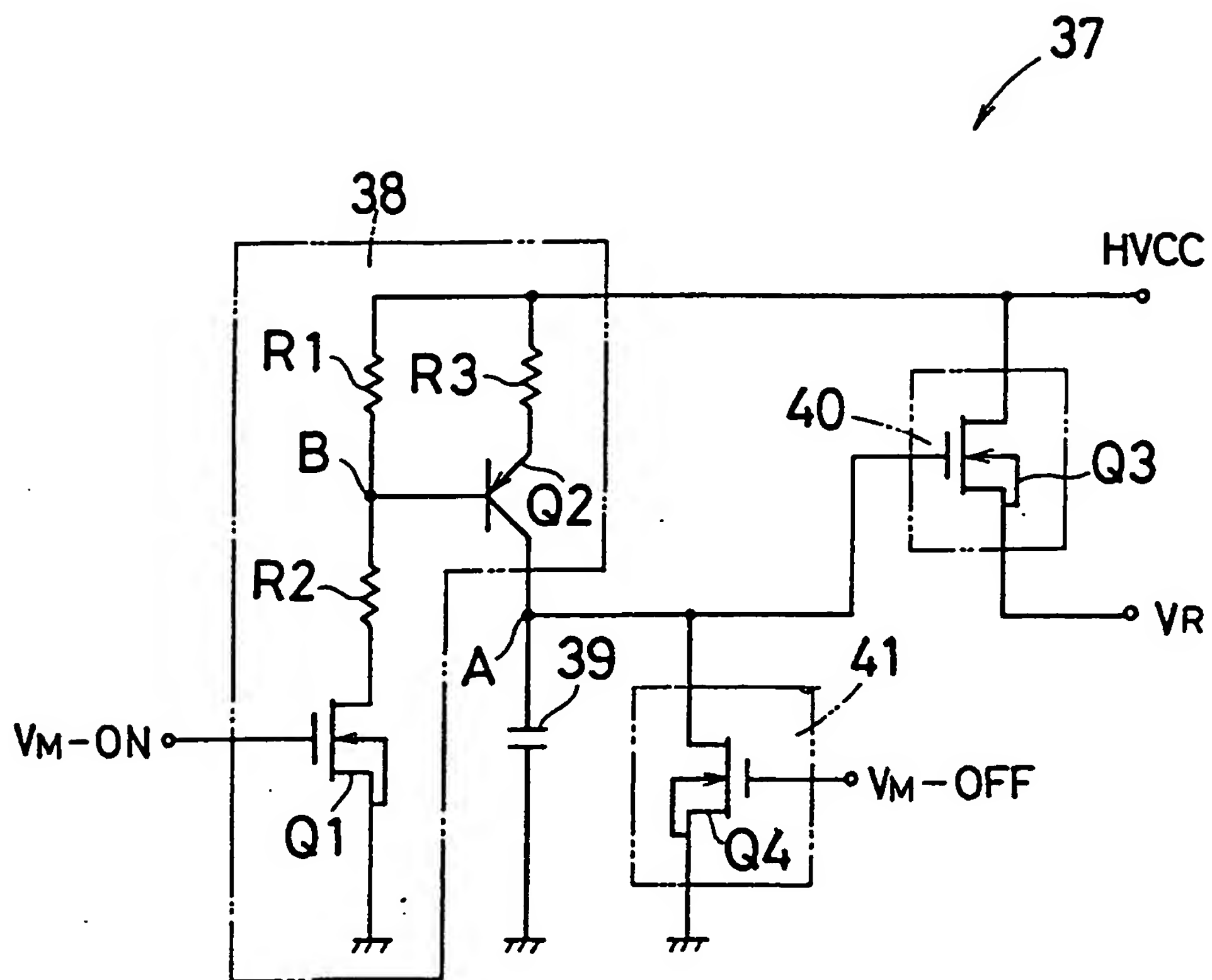


Fig. 15

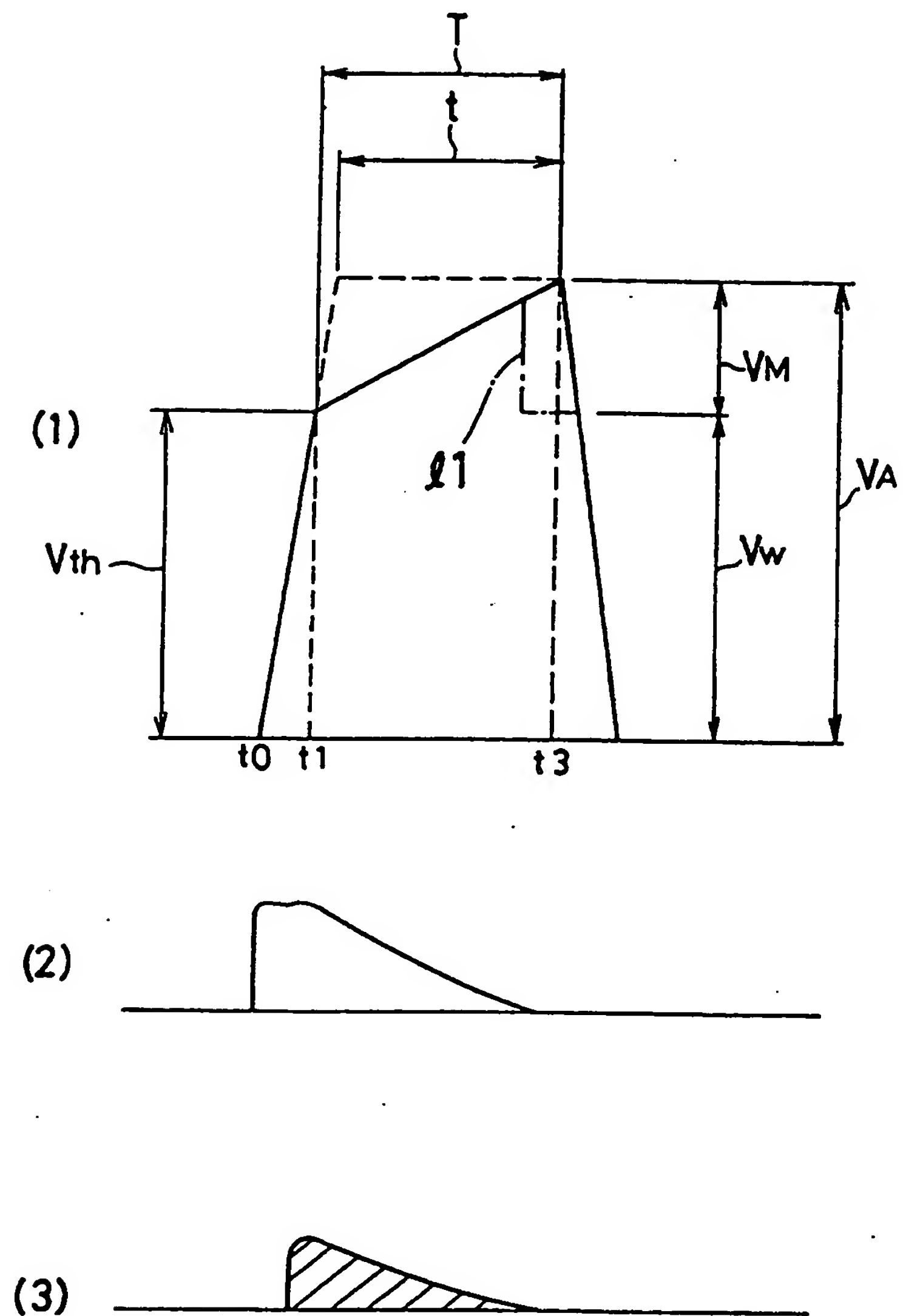


Fig.16

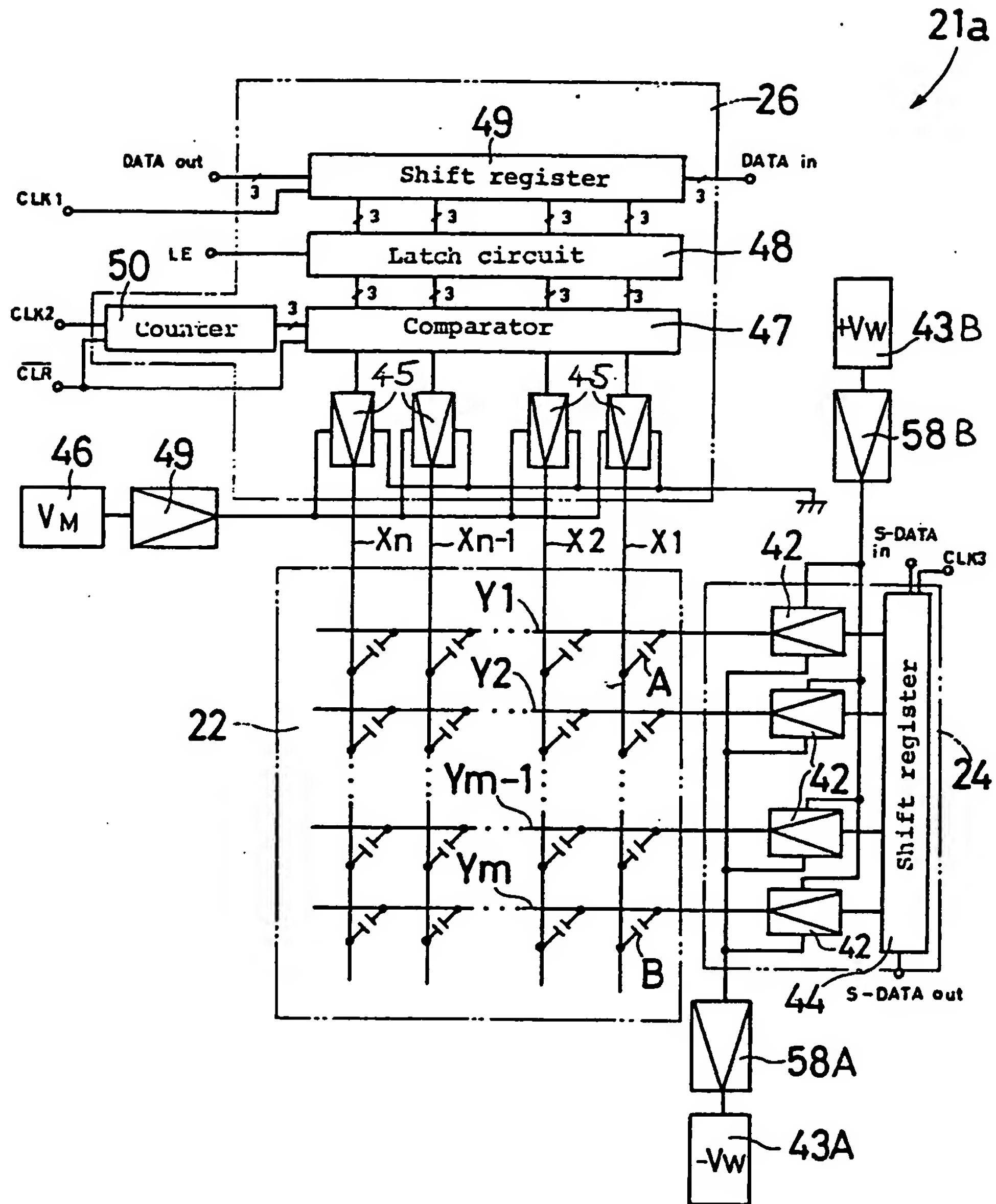


Fig.17

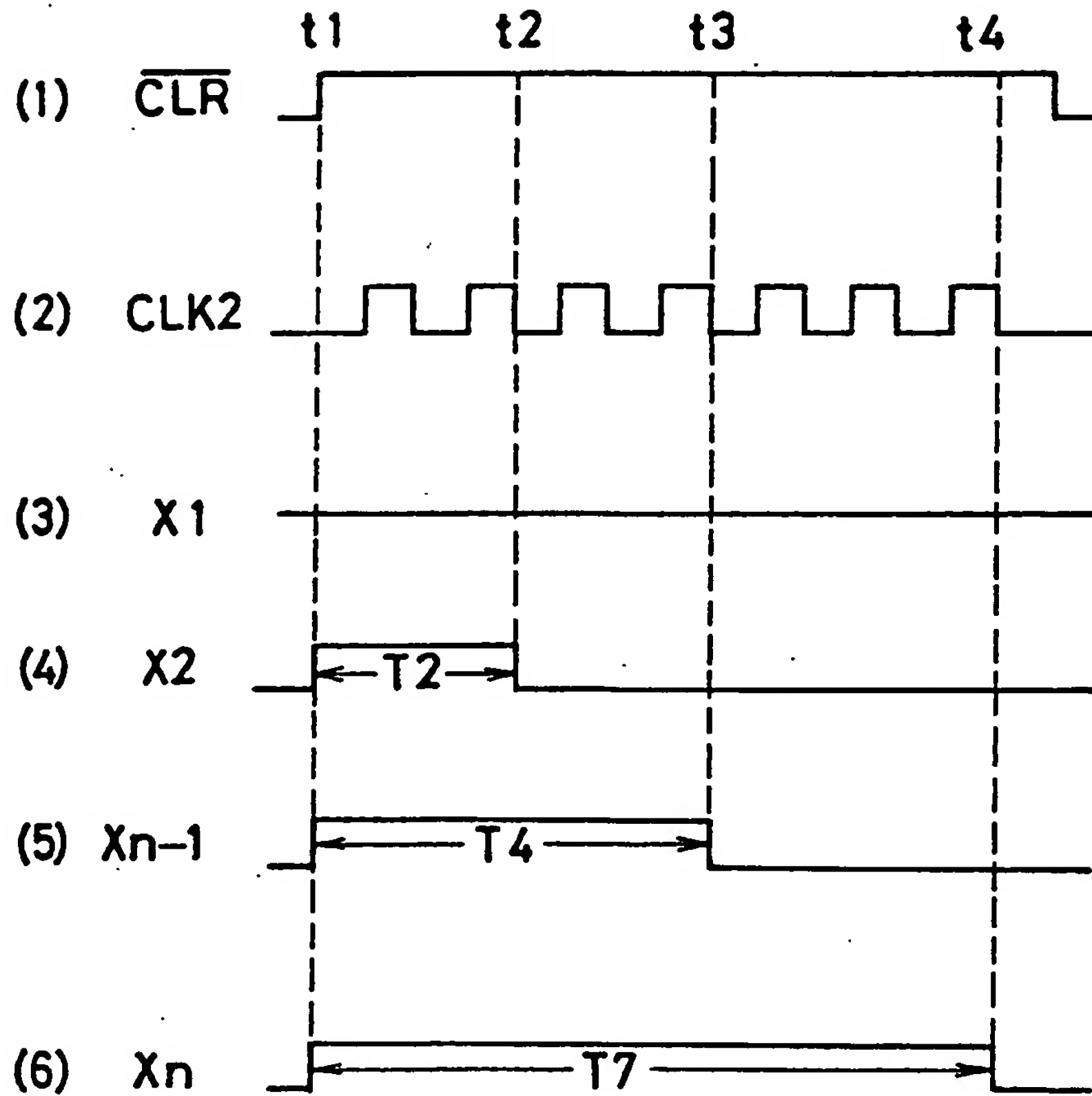


Fig.18

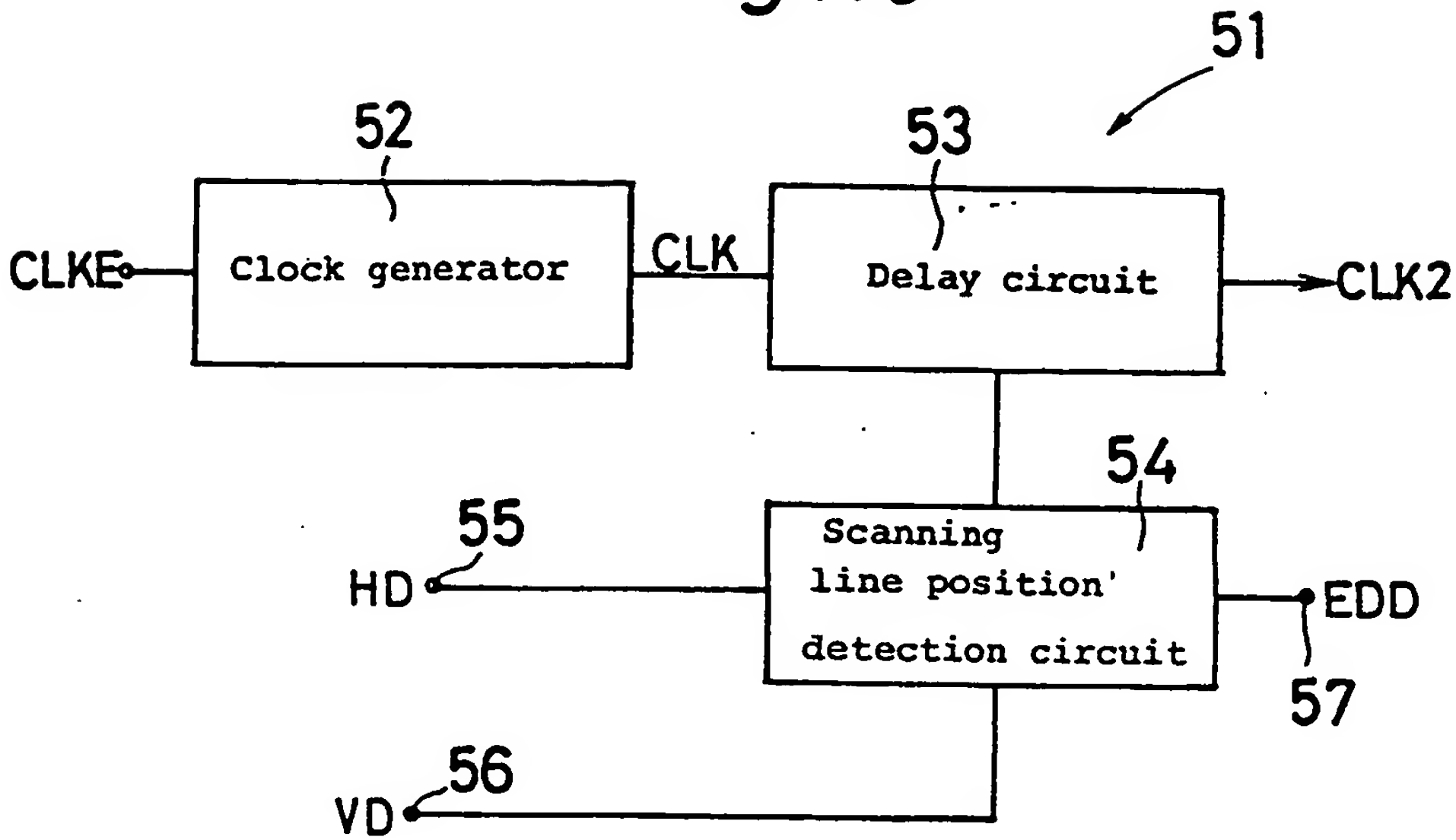


Fig.19

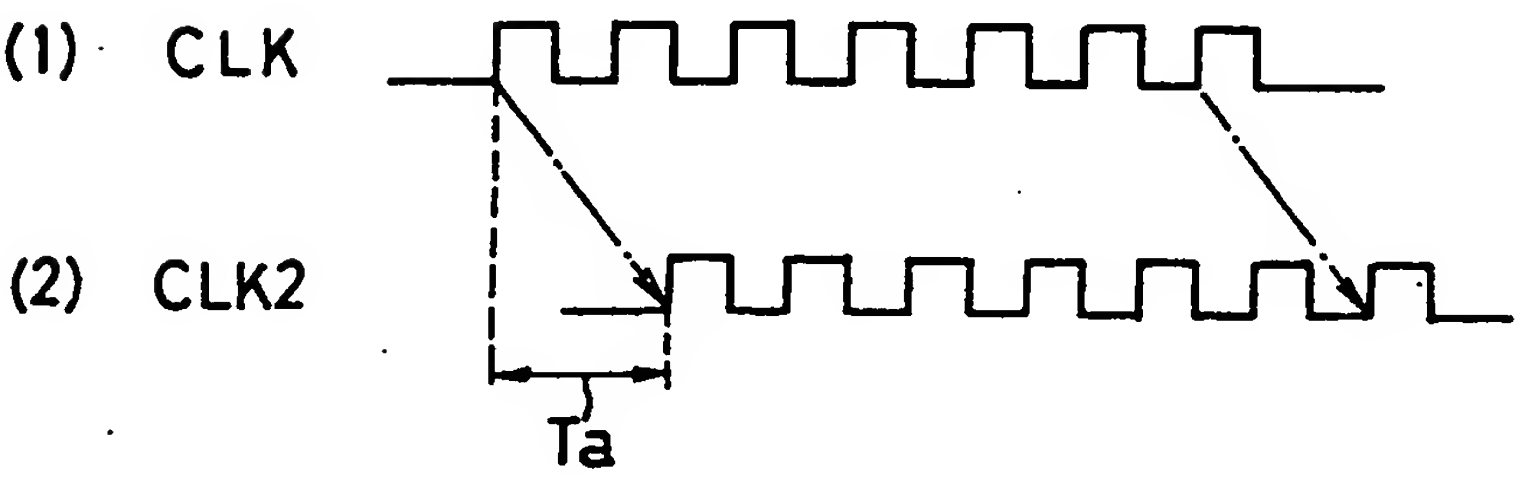


Fig.20

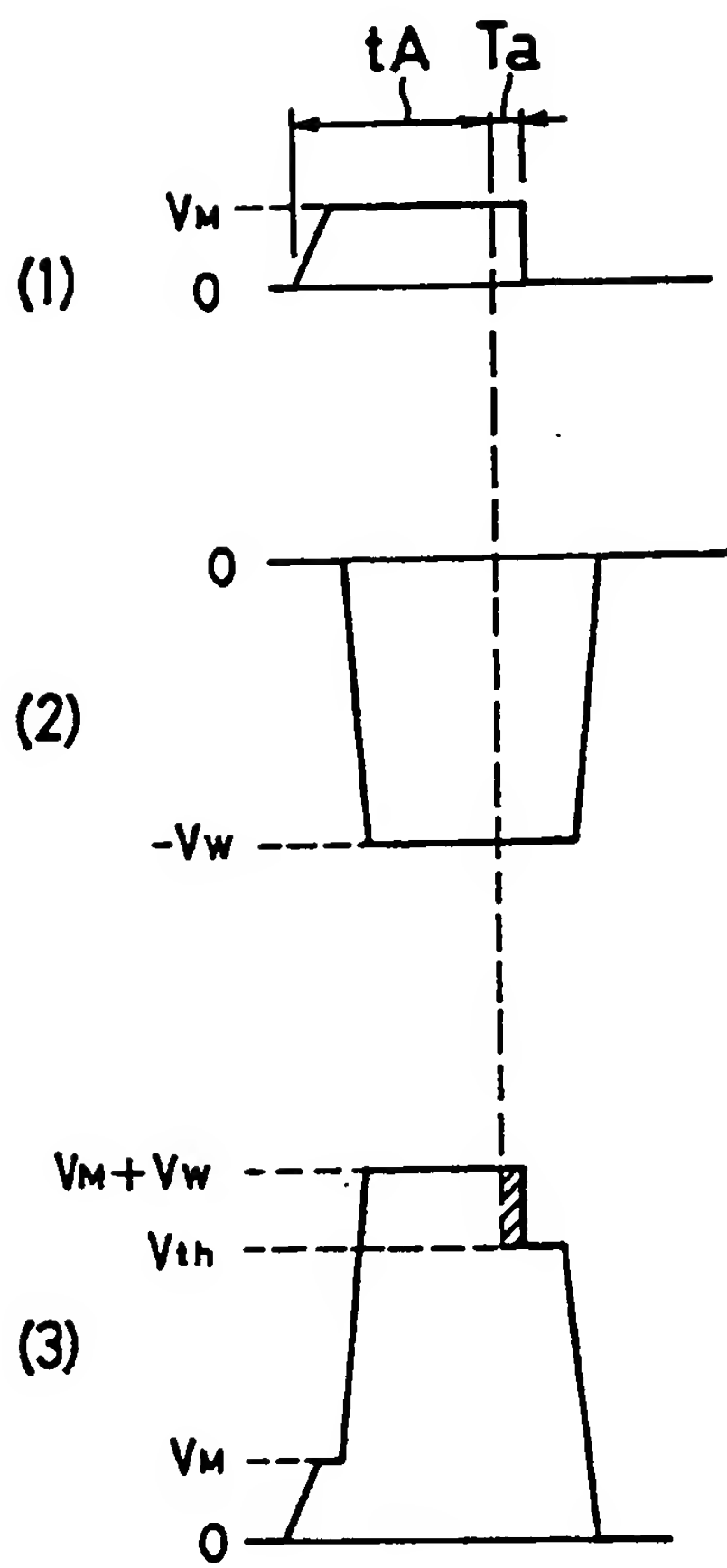


Fig.21

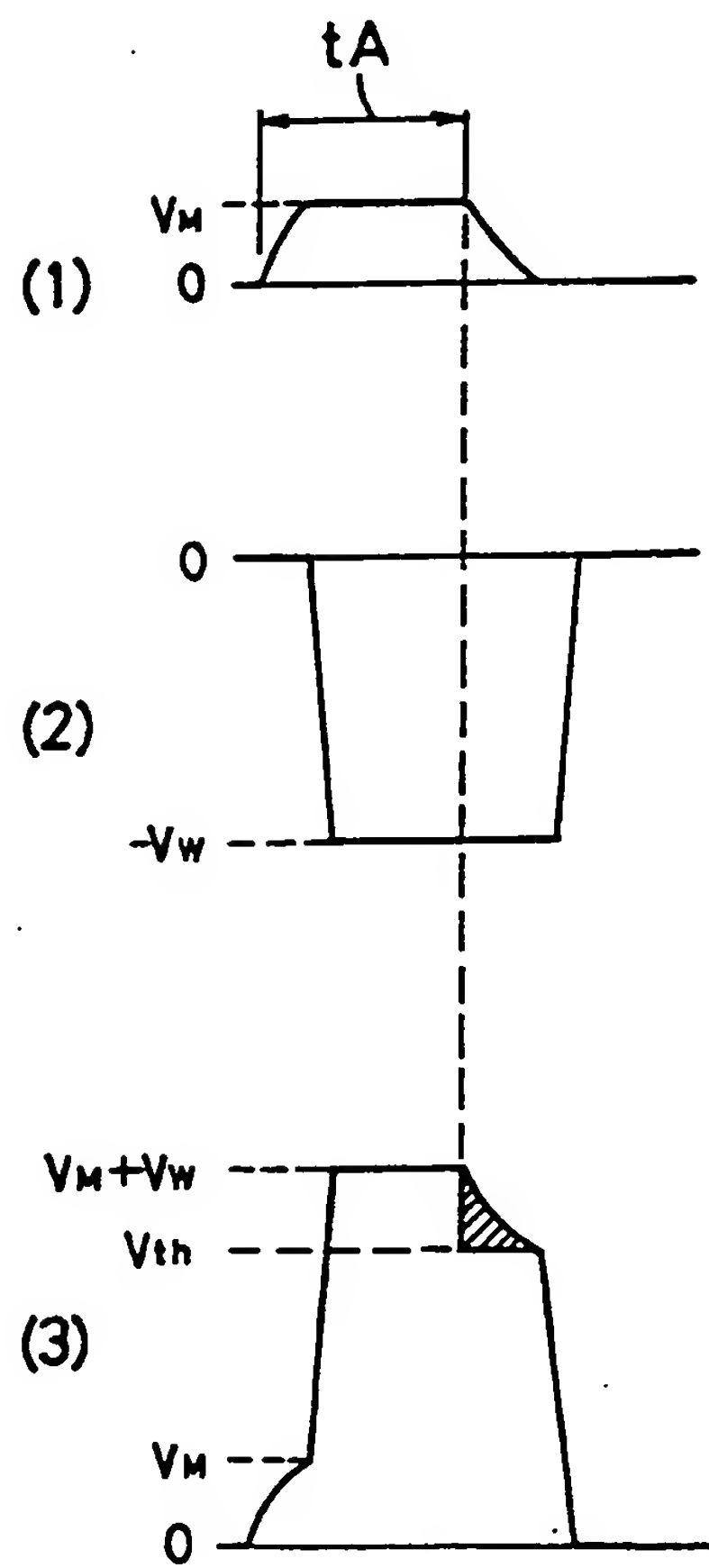


Fig. 22

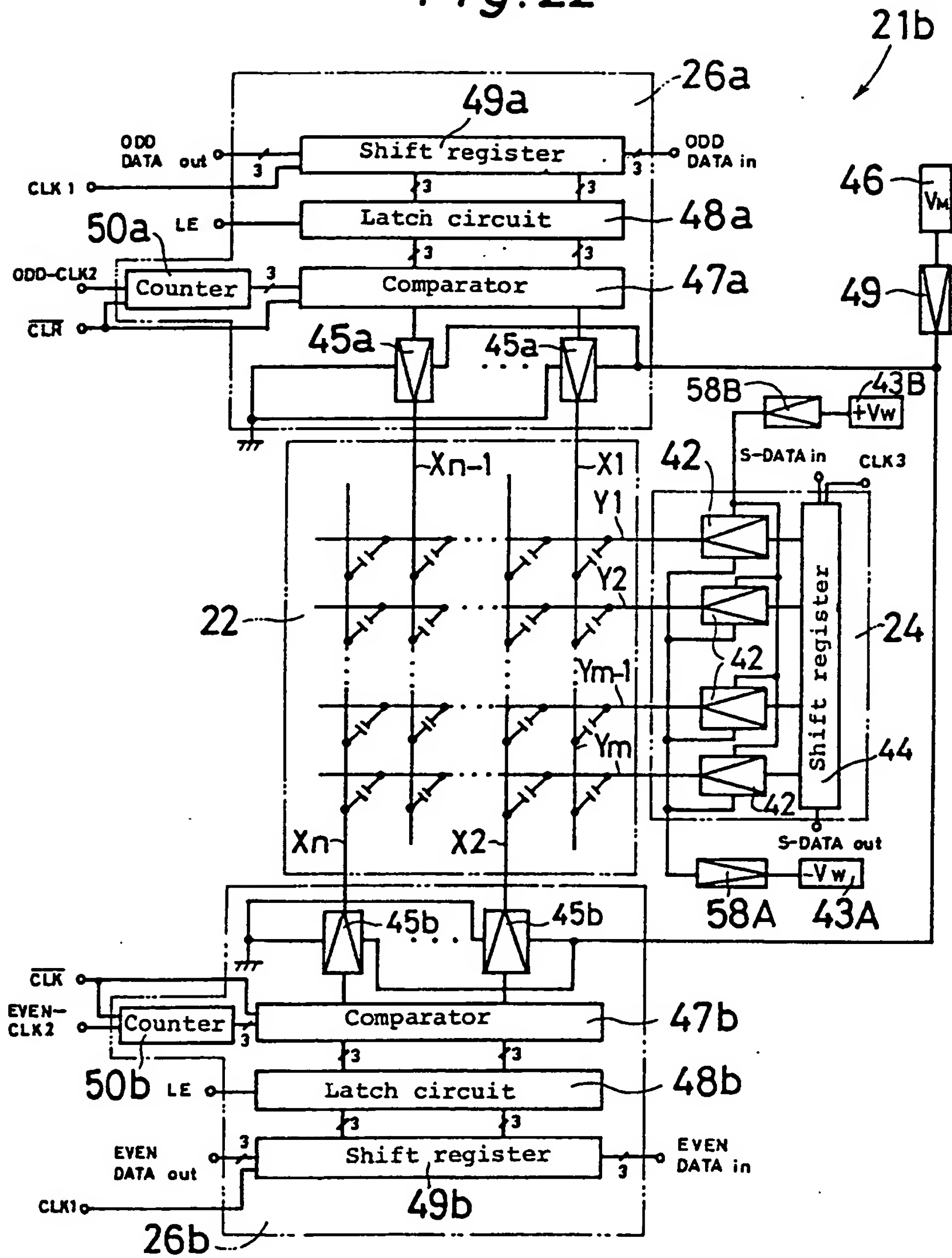
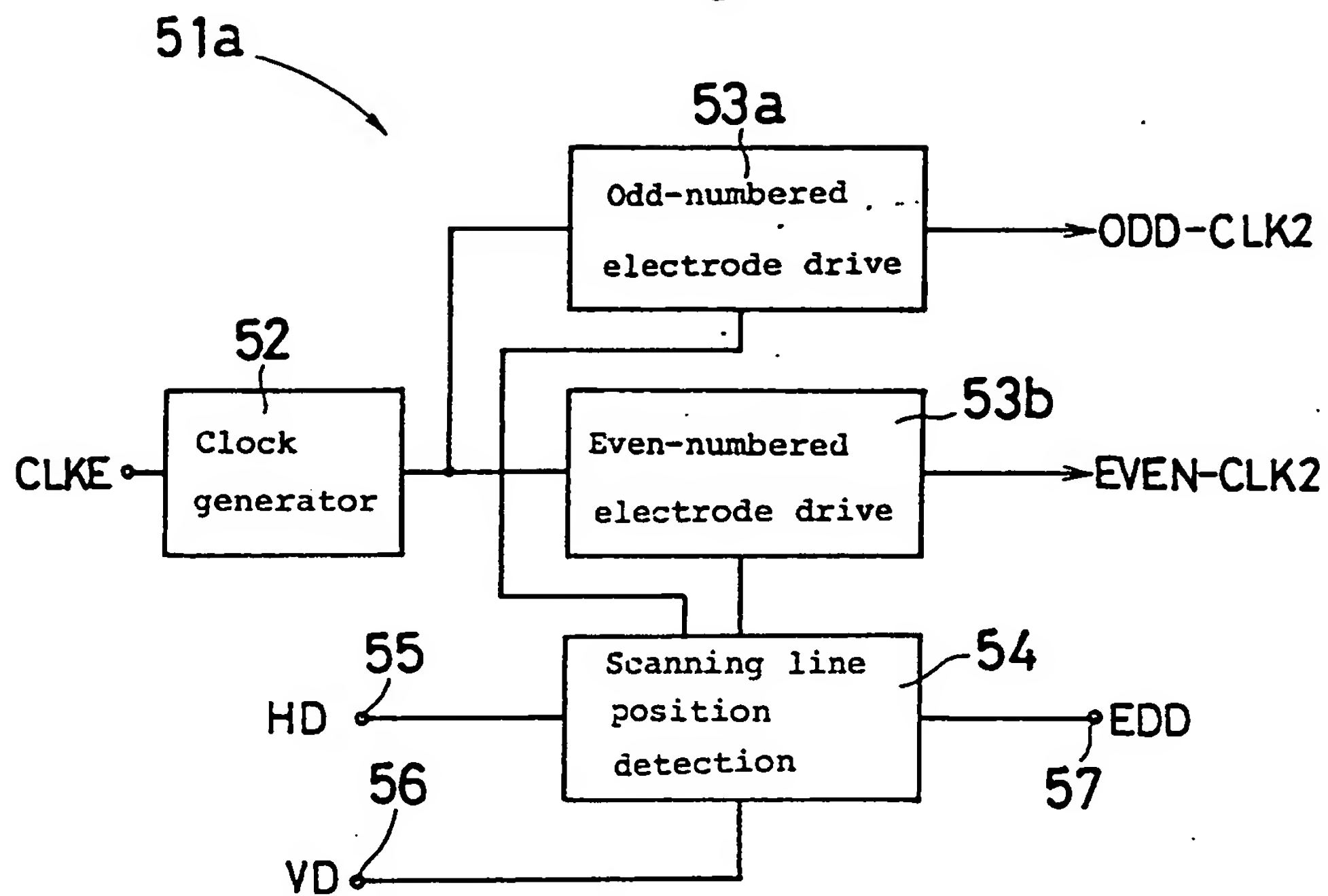


Fig. 23*Fig. 24*